GE Healthcare

MAC™ 5500

Resting ECG Analysis System

Service Manual

2020299-020 Revision E

The information in this manual only applies to MAC 5500 Resting ECG Analysis Systems with product code SCD. It does not apply to earlier software versions. Due to continuing product innovation, specifications in this manual are subject to change without notice.

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1 Introduction

For your notes

Manual Information

Revision History

Each page of the document has the document part number and revision letter at the bottom of the page. The revision letter identifies the document's update level. The revision history of this document is summarized in the table below.

Table 1. Revision History, PN 2020299-020

Revision	Date	Comment
A	25 July 2005	Initial release of this document.
B	14 December 2006	Added FRUs for MobileLink Silex serial server and HHP Model 4600 barcode reader.
C	18 October 2007	Items added to the FRU list.
D	10 October 2008	Added -007 board, 009C SD Card and -002 Comm PC board. Included Functional Checkout Procedure.
E	08 January 2010	Added CAM 14 Assembly V2 in Appendix C

Manual Purpose

This manual supplies technical information for service representative and technical personnel so they can maintain the equipment to the assembly level. Use it as a guide for maintenance and electrical repairs considered field repairable. Where necessary the manual identifies additional sources of relevant information and or technical assistance.

See the operator's manual for the instructions necessary to operate the equipment safely in accordance with its function and intended use.

Intended Audience

This manual is intended for the person who uses, maintains, or troubleshoots this equipment.

Warnings, Cautions, and Notes

The terms danger, warning, and caution are used throughout this manual to point out hazards and to designate a degree or level or seriousness. Familiarize yourself with their definitions and significance.

Hazard is defined as a source of potential injury to a person.

Term	Definition
DANGER	Indicates an imminent hazard which, if not avoided, will result in death or serious injury.
WARNING	Indicates a potential hazard or unsafe practice which, if not avoided, could result in death or serious injury.
CAUTION	Indicates a potential hazard or unsafe practice which, if not avoided, could result in minor personal injury or product/property damage.
NOTE	Provides application tips or other useful information to assure that you get the most from your equipment.

Safety Messages

Additional safety messages may be found throughout this manual that provide appropriate safe operation information.

DANGER
Do not use in the presence of flammable anesthetics.

WARNINGS
This is Class 1 equipment. The mains plug must be connected to an appropriate power supply.

Operate the unit from its battery if the integrity of the protective earth conductor is in doubt.

CAUTIONS
This equipment contains no serviceable parts. Refer servicing to qualified service personnel.

U.S. Federal law restricts this device to the sale by or on the order of a physician.

Responsibility of the Manufacturer

GE Medical Systems *Information Technologies* is responsible for the effects of safety, reliability, and performance only if:

- Assembly operations, extensions, readjustments, modifications, or repairs are carried out by persons authorized by us.
- The electrical installation of the relevant room complies with the requirements of the appropriate regulations.
- The equipment is used in accordance with the instructions for use.

General

The intended use of this device is to record ECG signals from surface ECG electrodes. This device can analyze, record, and store electrocardiographic information from adult and pediatric populations. This data can then be computer analyzed with various algorithms such as interpretive ECG and signal averaging for presentation to the user.

This device is intended for use under the direct supervision of a licensed health care practitioner.

Failure on the part of the responsible individual, hospital, or institution using this equipment to implement a satisfactory maintenance schedule may cause undue equipment failure and possible health hazards.

To ensure patient safety, use only parts and accessories manufactured or recommended by GE Medical Systems *Information Technologies*.

Contact GE Medical Systems *Information Technologies* for information before connecting any devices to this equipment that are not recommended in this manual.

If the installation of this equipment, in the USA, will use 240 V rather than 120 V, the source must be a center-tapped, 240 V, single-phase circuit.

Parts and accessories used must meet the requirements of the applicable IEC 60601 series safety standards, and/or the system configuration must meet the requirements of the IEC 60601-1-1 medical electrical systems standard.

The use of ACCESSORY equipment not complying with the equivalent safety requirements of this equipment may lead to a reduced level of safety of the resulting system. Consideration relating to the choice shall include:

- use of the accessory in the PATIENT VICINITY; and
- evidence that the safety certification of the ACCESSORY has been performed in accordance to the appropriate IEC 60601-1 and/or IEC 60601-1-1 harmonized national standard.

Equipment Symbols

For a list and examples of the symbols that appear on the equipment and packaging, refer to the MAC™ 5500 Resting ECG Analysis System Operator's Manual (PN 2020299-153).

Service Information

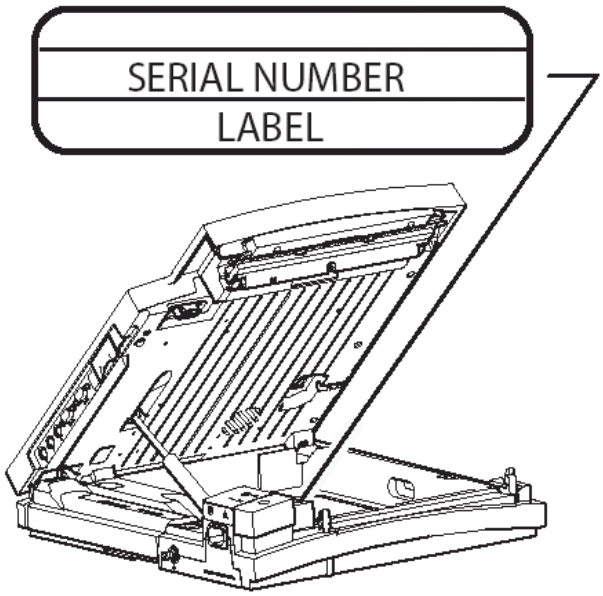
Service Requirements

Refer equipment servicing to GE Medical Systems *Information Technologies* authorized service personnel only. Any unauthorized attempt to repair equipment under warranty voids that warranty.

It is the user's responsibility to report the need for service to GE or to one of their authorized agents.

Equipment Identification

The serial number label is located inside the device where shown below.



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Every GE Medical Systems *Information Technologies* device has a unique serial number for identification. The serial number is formatted as shown in "Serial Number Format" on page 1-9.

NOTE

The examples shown are representative only. Your product label may differ.

Serial Number Format

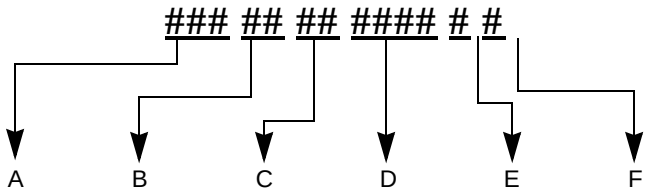


Table 2. Serial Number Format

A	[1]Product code
B	Year manufactured (00-99) 00 = 2000 01 = 2001 02 = 2002 (and so on)
C	Fiscal week manufactured
D	Production sequence number
E	Manufacturing site
F	Miscellaneous characteristic

1. This manual applies to MAC 5500 with product code **SCD.**

Label Format

Table 3. Equipment Identification Label

A	Date of manufacture in YYYY-MM format
B	Part number of product
C	Product code description
D	Serial number (described above)
E	Manufacturing site

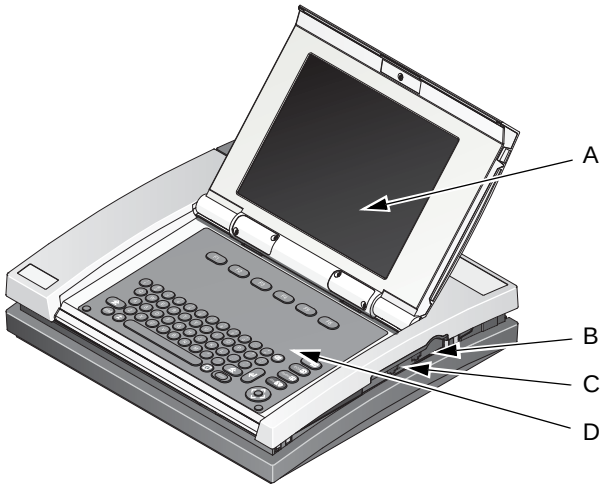
2 Equipment Overview

For your notes

General Description

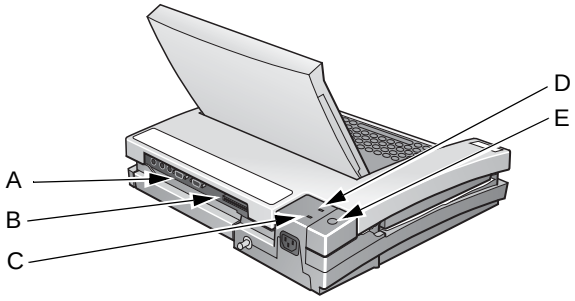
The MAC™ 5500 resting ECG analysis system is a 15 lead, 12 channel system with a 10.4 inch (264 mm) diagonal display, active patient cable, battery operation, and late potential electrocardiography. There are also options for communication capabilities.

Front View



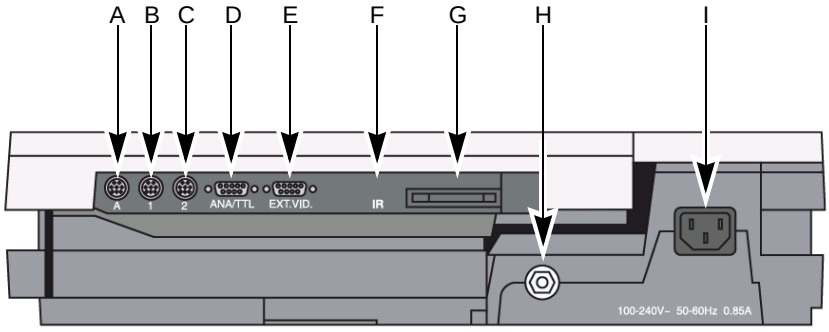
	Name	Description
A	display screen	View the waveform and text data.
B	modem port	Connect the telephone cable here.
C	LAN port	Connect to the LAN here. ■ The green LED right of this port indicates that power is supplied to the communication card from the Ethernet link. ■ The amber LED left of this port flashes to indicate network traffic.
D	keyboard	Press the keyboard keys to control the system or to enter data.

Back View



	Name	Description
A	back panel connectors	Connect peripheral devices here.
B	secure data card slot	Insert secure data card for external storage here.
C	green AC power light	Indicates the system is connected to AC power.
D	amber battery light	Indicates the battery is recharging.
E	internal access button	Press to open the system to change paper or the battery.

Connector Identification



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WARNING
LEAKAGE CURRENT – Keep leakage current within acceptable limits when connecting auxiliary equipment to this device.

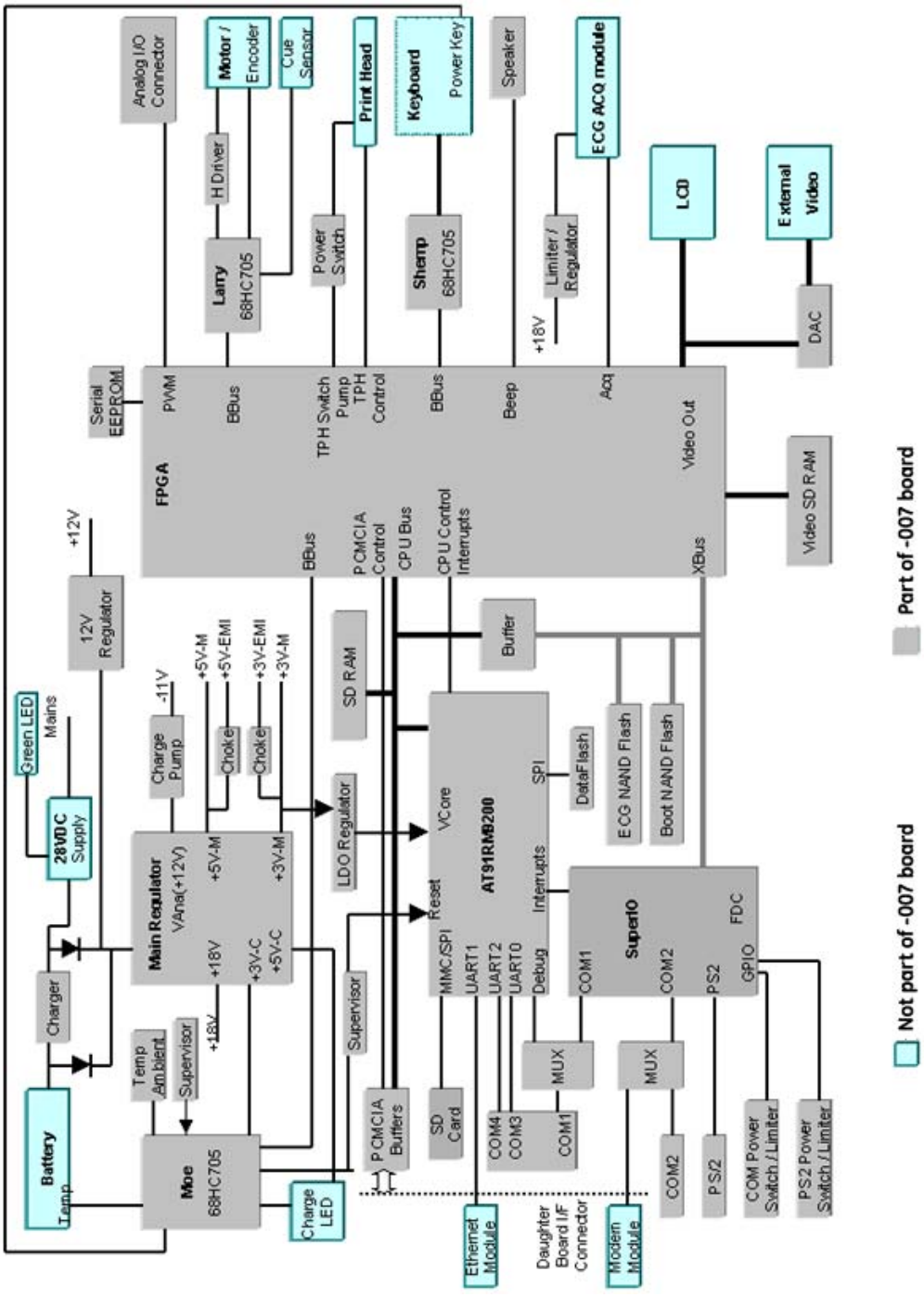
Total system leakage current must not exceed 300 microamperes (United States) or 500 microamperes (international).

Table 4. Back Panel Connectors

Item	Name	Description
A	A	Connect an optional card reader or optional bar code reader
B	1	Connect a GE KISS pump. (If system has the stress option, connect a T2000 or external blood pressure device cable to this port.)
C	2	Connect a local transmission cable, serial line, modem, or client bridge (wireless option).
D	ANA/TTL	Connect a device requiring analog data or TTL trigger (ultrasound, stress echo, ergometer, analog treadmill, blood pressure units, etc.).
E	EXT.VID.	Connect an external video display.
F	IR	Point at a MAC 5000, MAC 5500 or MUSE system's IR transceiver to transmit or receive ECG data.
G	card slot	Insert the system card into this slot to archive or restore data from external media or to update software.
H	ground lug	Connect non-grounded peripheral devices to ensure equipotential.
I	main AC power	Insert the main AC power cable.

MAC 5500 Block Diagram

Following is the basic diagram of the MAC 5500 with the 007 board. For additional information, refer to “Overview / Block Diagram” on page 2-7.



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Theory of Operation

Overview / Block Diagram

The MAC 5500 CPU board contains all of the circuitry for the MAC™ 5500 resting ECG analysis system except for the line power supply, acquisition module, keyboard and display. Although the MAC 5500 runs software derived from products based on the Max-1 architecture (running on the C-Exec operating system), it has almost nothing in common with that hardware family. Component references in this section are relative to the 801212-007 CPU board assembly.

The CPU board assembly contains the following:

- 64 MB SDRAM (holds both code and data)
- 32 MB SDRAM acts as video frame memory
- 32 MB NAND Flash (holds FPGA configuration and system code)
- 32 MB NAND Flash for ECG Record storage
- 128 KB Boot Data Flash (holds primary boot image)
- CRT video DACs
- External 12 Volt Power Switch
- Acquisition Module Transceiver / Power Switch
- Printhead Power Switches and Pixel Test Circuit
- Daughter Board Interface which support LAN and modem.
- Switch Mode Power Supplies
  - 3.3 Volt for Logic, LCD
  - 5 Volt for Logic, Printer
  - 12 Volt for LCD backlight, External Com Port Power
  - Battery Charger
  - -12 Charge Pump for Analog Circuits
- Linear Power Supplies
  - 1.8 Volt (AT91RM9200 Core and FPGA Core)
  - 2.5 Volt Reference
  - 3.3 Volt for System Supervisor (Moe Stooge)
  - 12 Volt for Analog Circuits
- Crystals / Clocks
  - 24 MHz Oscillator for FPGA
  - 32.768 Khz Real Time Clock for Super IO chip.
  - 32.768 Khz (AT91RM9200)
  - 18.432 Mhz (AT91RM9200)
  - 4 Mhz (3 devices, 1 for each Stooge)
- Atmel AT91RM9200 CPU Containing:
  - Incorporates the ARM920T™ ARM® Thumb™ Processor
    - 200 MIPS at 180 MHz, Memory Management Unit
    - 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
    - In-circuit Emulator including Debug Communication Channel
    - Mid-level Implementation Embedded Trace Macrocell (256-ball BGA Package Only)
  - Low Power: 30.4 mA on VDDCORE, 3.1 mA in Standby Mode
  - Additional Embedded Memories
    - 16K Bytes of SRAM and 128K Bytes of ROM

- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, Burst Flash, Glueless Connection to CompactFlash®, SmartMedia™ and NAND Flash
- System Peripherals for Enhanced Performance:
  - Enhanced Clock Generator and Power Management Controller
  - Two On-chip Oscillators with Two PLLs
  - Very Slow Clock Operating Mode and Software Power Optimization Capabilities
  - Four Programmable External Clock Signals
  - System Timer Including Periodic Interrupt, Watchdog and Second Counter
  - Real-time Clock with Alarm Interrupt
  - Debug Unit, Two-wire UART and Support for Debug Communication Channel
  - Advanced Interrupt Controller with 8-level Priority, Individually Maskable Vectored Interrupt Sources, Spurious Interrupt Protected
  - Seven External Interrupt Sources and One Fast Interrupt Source
  - Four 32-bit PIO Controllers with Up to 122 Programmable I/O Lines, Input Change Interrupt and Open-drain Capability on Each Line
  - 20-channel Peripheral Data Controller (DMA)
- Multimedia Card Interface (MCI)
  - Automatic Protocol Control and Fast Automatic Data Transfers
  - MMC and SD Memory Card-compliant, Supports Up to Two SD Memory Cards
- Three Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I 2 S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver/Transmitters (USART)
  - Support for ISO7816 T0/T1 Smart Card
  - Hardware and Software Handshaking
  - RS485 Support, IrDA Up To 115 Kbps
  - Full Modem Control Lines on USART1
- Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, 4 External Peripheral Chip Selects
- Two 3-channel, 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability

- FPGA Containing:
  - XBus Controller
  - LCD Controller with SDRAM Frame Buffer.
  - Video Waveform Scroller
  - Interrupt Controller
  - System Interrupt Generator
  - Acquisition Module Interface
  - Thermal Printhead Interface
  - Serial EEPROM Interface
  - BBus Controller
  - Four PWM Analog Outputs
  - Beep Generator
  - PC Card Interface

- A PC Super I/O controller containing:
  - Two Serial Ports (one dual mode RS-232 / IrDA)
  - Clock/Calendar (Y2K compliant)
  - PS-2 Keyboard Port (for card and barcode readers)
  - Floppy Disk Controller

- Three Peripheral Microcontrollers (The Three Stooges):
  - System Supervisor / Battery Charger-Gauge (Moe)
  - Printer Motor Controller / Analog Input (Larry)
  - Keyboard Interface (Shemp)

Power Supplies

The MAC™ 5500 resting ECG analysis system requires several regulated voltages for operation of its various components. The Main Regulator provides most of the supply rails. The supply rails are:

+3V-C

MAC™ 5500 resting ECG analysis system is never truly “off.” The system supervisor microcontroller (MOE) must constantly monitor the power key and perform battery charging/gauging. The clock/calendar in the Super I/O chip must also maintain time/date when the machine is off. These functions are powered from the +3V-C rail, which provides power continuously from the battery pack regardless of the state of the rest of the system. The Main Regulator produces +3V-C directly from the battery rail via an internal low current linear regulator. Only 5mA are available from +3V-C, so it must be used sparingly.

NOTE

The MAX782’s low current regulator is dreadfully inefficient. Regulator Q current appears to be about 3x the load current. This makes conservation of load on +3V-C crucial.

+3V-M

Most of the MAC 5500 hardware runs from +3V-M. The MAX782 provides this rail from the battery via a PWM synchronous switching regulator. Moe controls +3V-M in tandem with +5V-M.

+3V-EMI

This is simply an RF blocked feed from +3V-M. +3V-M load is contained within the CPU board. Power for devices for external functions is supplied by +3V-EMI. The isolation of +3V-EMI from +3V-M may be unnecessary as the concept has never been tested for its effect.

+5V-M

The MAC™ 5500 resting ECG analysis system is not fully in the 3V age. The Super I/O and thermal printhead require 5V power. The MAX782 provides this rail via another PWM synchronous switching regulator. Moe controls +5V-M in tandem with +3V-M.

+5V-EMI

Similar to +3V-EMI, this rail is an RF blocked feed from +5V-M, used to power devices for external functions. The isolation of +5V-EMI from +5V-M may be unnecessary as the concept has never been tested for its effect.

+18V

The Main Regulator's 5V switching output also supports generation of a non-regulated 18V rail, which is used to provide power for the acquisition module. By providing the acquisition module with 11.5V linearly regulated power from the +18V rail of the main regulator rather than the main 12V regulator (U17), acquisition is not affected by excessive current draw from the printer motor or external loads on the COM ports (esp. KISS pump). The acquisition module's power requirements are modest, so efficiency is not a pressing concern and the lower efficiency of this approach is acceptable.

+1.8V

The Atmel CPU and FPGA (Xilinx Spartan 2) operates their internal core logic at 1.8V, while their I/O ring runs at the system standard 3.3V. The 1.8 Volt regulator, a low dropout linear regulator, drops +3V-M to 1.8V for use as a core supply.

+12V

The paper motor drive circuit, LCD backlight and external COM ports all require 12V. The Main Regulator's 18V output cannot provide sufficient current for all of the systems 12V loads, so a secondary 12V regulator is required. The Main 12V Regulator (U17), a switching buck regulator, provides the higher currents needed by these loads. A P-channel MOSFET (Q1) switch precedes the regulator to provide on/off control. Gate capacitor C12 slows the turn on/off time of the MOSFET switch to eliminate switching transients. The voltage divider created by R133,134 prevents the full supply rail from being impressed across Q1's gate when on. This protection is necessary, as the maximum Vgs of the MOSFET is less than the peak supply voltage.

REF2V5

The high power rails are neither precise nor quiet enough to be used as the reference for analog input/output or internal measurement circuits. The Analog Reference Regulator (U50), a 2.5V shunt regulator provides a quiet and stable reference voltage for such purposes. VREF is derived from +5V-EMI rather than +3V-EMI to minimize the change in reference current with changes in input rail voltage. The difference between 5V and 2.5V is three times greater than the difference between 3.3V and 2.5V. If the absolute ripple on both supplies is the same, the modulation of reference current will be 3 times less if power is derived from +5V.

VAna+, VAna-

The analog output circuitry is powered by a low current switched 12V rail, provided by the Main Regulator. VAna+ provides the positive supply for the output op-amps. A charge pump voltage inverter is provided to produce an approximate -11V rail for the op-amps. Although only the ECG output is bipolar, all output amplifiers are driven from VAna-. A short circuit on either of the unipolar DC outputs could load VAna- sufficiently to affect the negative peak swing of the ECG output. The ECG and DC outputs are not required to operate correctly in the presence of abnormal loads.

Clocks

Super I/O and FPGA

Both of these devices uses the 24 Mhz clock oscillator Y5 to drive their internal requirements for various clock frequencies. The main function of the Super I/O IC is for serial port communication and real time clock; all the needed timing comes from this oscillator. The FPGA provides many functions including the acquisition interface, the printer interface, and the Stooges interface (Bbus) to name a few. The FPGA uses a built-in frequency doubler to raise this 24 Mhz clock to 48 Mhz for internal use. All functions inside the FPGA use the clocks derived from 48MHz. The main derived clocks are:

- 1 MHz for acquisition interface
- 4 MHz for printer data shift clock interface.
- 4 MHz for EEPROM data shift clock
- 24MHz for VGA LCD panel clock.

The VGA LCD controller, that include the SDRAM frame buffer controller use 59.904 MHz external memory clock from ATMEL CPU in addition to the 48MHz FPGA clock

CPU ATMEL AT91RM9200

The ATMEL AT91RM9200 has two oscillators. Slow Clock oscillator and Main Oscillator. The Slow Clock Oscillator uses 32,768 KHz crystal for clock generation. The CPU runs in Slow Clock mode (@48MHz) after system reset. Slow clock is also used by the built in RTC. The CPU does not use the ATMEL RTC for the system timing requirements. The Main oscillator uses 18.432 MHz crystal. Processor clock (179.712 MHz), Master clock (59.904) for external Bus Interface and Peripheral Clocks are derived from main oscillator by the Master Clock Controller.

CPU (Stooges)

Each of the three Stooges has its own 4 Mhz ceramic resonator for use in generating their respective clocks.

RTC

The Real Time Clock of the system is provided as a part of the Super I/O controller. The timing for this function is derived from its own 32.768 Khz crystal.

CPU

The ATMEL AT91RM9200 replaces the Strong ARM SA1110 used in -005 board. The AT91RM9200 uses high performance, low power consumption and high code density ARM920T processor core. One of the major difference between SA1110 and AT91RM9200 is the absence of built in LCD controller and 16-bit static memory controller. StrongARM support 32 bit memory interface. The Processor Clock and External Bus speed is limited to 180 and 80 MHz when compare with the 206 and 103 MHz of StrongARM. Having an external LCD controller with a separate video memory interface compensates overall performance of the CPU.

External Bus Interface

The external bus interface width is limited to 16bit in ATMEL CPU when compare with the 32 bit interface of StrongARM. All the non VGA FPGA registers are either 8 bit or 16 bit wide. However all these were accessed using 32 bit access in -005 board and aligned to 32 bit word. To port the applications that was written for the 32 bit access, all the Non VGA memory space within the FPGA are accessed in 32 bit mode in -006 board. When the ATMEL static memory controller see a 32 bit memory access, it perform two consecutive 16 bit access. To avoid over writing of FPGA register with upper 16-Byte data, The FPGA register access logic is designed in such a way that, the FPGA ignores upper 16 byte access. However for access to the pixel data FIFO, the upper 16 bit contains valid data and the this will be loaded into the next 16 bit word.

The VGA registers are accessed using 32 bit access. The Frame Buffer area can be accessed either in 32 bit word mode or byte mode.

Boot Loader

In the -005 board, after power ON, the FPGA gets configured using the micro controller Curly. The FPGA emulate the boot ROM and the start up code was placed in the Boot ROM from the smart media card by the micro controller Curly.

The ATMEL AT91RM9200 has built in boot program in the internal ROM. The -006 and -007 boards utilize the ATMEL CPU itself for bringing up the board. Since the service of Curly is no longer required, it is removed from the board. At power ON if the BMS pin is high, ATMEL starts executing boot code in the internal ROM. The boot program looks for valid code in SPI data flash (U66) and, if found, downloads the program into SRAM and starts executing from SRAM after remap. The -006 and -007 boot program loads primary boot code into the SDRAM after initializing it. The primary boot program reads the PCB ID code from three port pins and then searches the NAND Flash for a matching FPGA configuration image (pages with ID “Xn” where n is the 3-bit PCB ID code 1-8 plus one). Once located, the configuration image is loaded into the FPGA in fly-by fashion. Blinking of LED DS3 at 1 Hz indicates successful completion of FPGA configuration. The primary boot program then loads the secondary boot code from NAND to SDRAM and transfers the control to the secondary boot program. Buffer U55 is used to get the direct CPU access to NAND Flash. To configure the FPGA in fly-by mode, the data needs to be present at the Xbus while toggling CCLK. This is achieved by toggling the NAND_RE* alternately with CCLK. The NAND_RE* needs to be under the GPIO control instead of static memory controller to do this. The ALE and CLE are also controlled in GPIO mode and tied to low level during read cycle while configuring the FPGA. The CLE and ALE acts as address line A23 and A25 respectively during Address and command cycle as well as access other than FPGA configuration. The reason for omitting A24 is because of AT91RM9200 silicon bug. The A24 does not work like an address pin. It can work only as GPIO line.

The primary boot code also contains the application for software update. If there is no valid code in the NAND FLASH, the primary boot code looks for SD Card and if detected it down load the code from the SD Card to NAND Flash and reset the system. If the primary boot code can not detect a valid code within 2 minutes 6 seconds, Moe shuts down the system. The status of software update is indicated on DS1 and DS2. The DS1 and DS2 are not visible once the top cover is in place. The Moe flashes amber charge LED at 1Hz to indicate that software update is in progress. But it can not provide the completion status. Refer the table below for the status messages from LEDs DS1 and DS2 during primary boot software update.

DS1 Red	DS2 (Green)	Status
Off	Flashing	No SD card detected for software updated
Off‘	On	Copying image files from SD card to SDRAM
Off	Off	Erasing and / or formatting the NAND Flash. Applicable only during the software update process.
On	Off	Programming the NAND Flash
Flashing	Flashing	Successful completion of programming
Flashing	Off	Error - Could program all the image files. But error in programming the status page 'Z0'.

DS1 Red	DS2 (Green)	Status
On	On	Error - Could not program all the image files as well as the status page 'Z0'.
On	Flashing	Error - Could not program all the image files. But the status page 'Z0' updated successfully

A copy of the primary boot program (pages with ID “Bn” where n is the 3-bit PCB ID code 1-8) is kept in NAND flash. This is updated whenever a software update happens. For -006 and -007 boards, the FPGA image and Primary boot code image ID’s are X3 and B3 respectively.

The primary boot program can do a forceful software update, even if a valid program is present in the NAND Flash, by using a special SD Card, which has a file, update.com, in the root directory. The service menu provides a provision to update the SPI data flash with the primary boot program copy residing the NAND Flash.

FPGA Internal Logic

All of the MAC™ 5500 resting ECG analysis system’s proprietary hardware is contained in a single Xilinx FPGA that contains:

- XBus Controller
- Video Interface
  - LCD Controller with SDRAM frame buffer
  - Video Waveform Scroller
- Interrupt Controller
- System Interrupt Generator
- Acquisition Module Interface
- Thermal Printhead Interface
- Serial EEPROM Interface
- BBus Interface
- Four PWM Analog Outputs
- Beep Generator

The following descriptions give an overview of the FPGA's functionality. For detailed information on the internal circuitry, refer to the schematic. For a programmer's eye view of the FPGA, see the source file "hardware.h". Where appropriate, circuitry external to the FPGA is also described.

Board ID Register

It is necessary to identify versions/revisions of the CPU board automatically in the field. The ATMEL primary boot code read the boot ID port pins to identify the FPGA image and startup code required for the board. The board ID register contains a hardwired three bit code that tracks the FPGA image number, indicating to the ATMEL just which FPGA image has been loaded. Three additional FPGA inputs are reflected in this register to allow further refinement of the board identity. Resistors (R98 and R99 through R129) are used to program the board ID.

Board ID Code	Versions of the 801212 CPU Board assembly
000h	-001, -002
001h	-003
002h	-004 (not used)
003h	-005
004h	not used
005h	-006
006h	-007

XBus Controller

To reduce loading on the high speed processor address and data busses, a slow speed byte bus is provided for peripheral interface. The Super I/O controller and NAND Flash ICs are both located on this bus. Unlike the 3.3V only main data/address busses, XBus is compatible with both 5V and 3.3V logic. To maintain software compatibility with previous board versions, the low order address byte is not used by XBus. Starting XBus addressing with A8 also produces Super I/O addresses that easily map to their standard PC equivalents (simply append 0x00 to a datasheet Super I/O address offset to get a MAC 5500 Super I/O address offset).

Video Interface

LCD Controller with SDRAM Frame Buffer

Continuing problems with LCD controller part obsolescence have made implementation of a controller design in the FPGA attractive. The MAC 5500 GUI software does not depend on sophisticated video functionality, so an FPGA implementation of a suitable display controller can be reasonably compact. By implementing the controller in the FPGA (using the VHDL hardware description language) obsolescence is avoided, and future upgrades are easily implemented.

The LCD controller is comprised of these functional blocks:

- Video Timing Generator (See "Video Timing" on page 2-17)
- SDRAM Frame Buffer Controller (See "SDRAM Frame Buffer Controller" on

page 2-17)

- Format pack/unpack logic (See "Format pack/unpack logic" on page 2-17)
- Line buffer (See "Line Buffer" on page 2-18)
- Fill Engine (See "Fill Engine" on page 2-19)
- Main State Machine (See "Main State Machine" on page 2-20)
- Interrupt management (See "Interrupt Management" on page 2-20)

Video Timing – The LCD controller generates video pixel and line timing from a global 60Mhz clock inside the FPGA. The timing generator consists of one counter for timing pixels within a line (including generation of horizontal sync, horizontal front and back porches, and LCD data enable timing) and another for timing lines with a frame (including generation of vertical sync, vertical front and back porches and generation of Line FIFO fill requests). In addition, the timing generator increments a memory address register by the line pitch (640) at the beginning of each video line, so the Line FIFO knows where to get the next line of pixels. The controller produces fixed timing for a 640x480 LCD, and requires no initialization to produce that timing. Support for future, higher resolution displays, can be obtained by modifying the source code for the controller itself, providing the most efficient hardware implementation possible.

SDRAM Frame Buffer Controller – The LCD obtains pixel data from a 1Mbyte region of a 32Mbyte, 16-bit wide synchronous DRAM (SDRAM). The SDRAM buffer is shared by the display controller and the CPU, allowing system software to directly manipulate screen pixels.

At power-up, SDRAMs must be configured for proper operation. Properties such as RAS/CAS latency and burst length are written into a control register in the SDRAM, and an initial burst of refresh cycles are performed to prepare the memory array for operations. The SDRAM controller does this all automatically at startup, requiring no initialization by the CPU.

SDRAMs, being dynamic, require periodic refresh to maintain the contents of the memory array. The SDRAM controller performs this refresh automatically between accesses. All details of SDRAM bank management and page boundary crossing are managed automatically in the SDRAM controller. In addition, through the use of pipelining, the SDRAM controller allows burst accesses to and from SDRAM at full memory speed. All details of burst cycle management, including setup and page boundary crossings, are handled transparently by the SDRAM controller. The SDRAM memory clock is derived from the CPU memory clock, and is passed out of the FPGA and back in to allow one of the FPGA's on-board DLLs to "zero out" all internal FPGA delays. This delay compensation allows the SDRAM controller to operate reliably at very high speeds (>= 100Mhz).

Format pack/unpack logic – The MAC 5500 display architecture is based on the division of pixels into static and dynamic planes. As discussed elsewhere, this technique allows the smooth scrolling of ECG waveforms across the screen while buttons, annotations and other graphics remain stationary. Previous generations of MAC 5000 display controllers packed the five bits of each static plane pixels into the same byte of memory as the three bits from the corresponding dynamic plane pixel. In that scheme, pixel manipulations required the CPU to read the combined pixel, modify either the static or dynamic component, and write the result back to memory. Such read-modify-write operations are time consuming.

In contrast, the FPGA implementation of the frame buffer takes advantage of SDRAMs high speed, large size, individual byte addressability, and 16-bit width, to

access both the static (5 bits) and dynamic (3 bits) portions of a pixel separately, and simultaneously. The SDRAM bus is effectively split into a “dynamic byte lane” and a “static byte lane”. The resulting improvement in drawing algorithm speed is substantial.

The 16-bit wide bus of the SDRAM allows each read/write cycle to access two bytes of data. During writes, upper and lower byte strobes allow independent writing of either or both bytes. During reads, both bytes are always presented. Unneeded read data bits are ignored by the CPU. The LCD controller takes advantage of the individual accessibility of the bytes to eliminate the need for the CPU to pack and unpack the static and dynamic pixels. At the expense of unused memory bits (a small expense as less than 1/16th of the entire SDRAM space is needed at all) the LCD controller maps the 5 bits of each static pixel into one SDRAM byte lane (the static lane), and the 3 bits of each static pixel into the other (the dynamic lane). Unused bits in each lane are written as zeroes, and ignored on reading.

On the CPU side, the SDRAM frame buffer appears as two regions, the static and dynamic planes. Each plane is a contiguous array of 480 lines of 640 pixels each. Within the static plane, the lower 3 bits (the dynamic bits) of each pixel byte are ignored on writes, and read as zeroes. Within the dynamic plane, the upper 5 bits of each pixel byte (the static bits) are ignored on writes and read as zeroes. The dynamic plane is located 1/2 Mbyte above the static plane and address bit A19 is used to differentiate between them. The interface from the LCD controller to the CPU is 16-bits wide, allowing two pixel bytes to be moved in each read/write cycle.

In the 16-bit wide SDRAM, each word (independently byte addressable) contains both a static and a dynamic pixel byte, each in their own lanes. When the CPU writes a pixel to the static plane, the upper five bits of the byte are routed to the static byte lane (the lower three bits are set to zero) and the dynamic byte lane is disabled. When the CPU reads a static pixel, both the static and dynamic byte lanes are accessed, but only the upper five bits of the static byte lane are passed on to the CPU (the lower three bits are zeroed). Access to the dynamic plane proceed in much the same manner, with the appropriate bits being routed to the dynamic byte lane while the static byte lane is disabled.

Because each 16-bit word of SDRAM contains one pixel, and each 16-bit access of the CPU into the frame buffer contains two, the LCD controller must pack/unpack pixels on the fly. During writes, if the CPU signals a single byte write, the LCD controller writes the byte onto the proper lane (as determined by A19) of one memory word. If the CPU signals a two byte write, the LCD controller queues a two cycle burst write into two consecutive words of SDRAM. On reads, the LCD controller always reads two pixels from memory and packs them into a single word for access by the CPU, which may use both pixels, or ignore one.

By design, SDRAMs are faster when data can be moved in sequential bursts. The Atmel ARM CPU asynchronous bus interface does not support burst accesses, so the opportunity to burst is limited. The LCD controller does take advantage of the 16-bit wide nature of the asynchronous bus to allow bursts of two pixels into and out of memory when possible. This nearly doubles frame buffer bandwidth over a byte-at-a-time interface. Finally, as mentioned previously, the CPU is able to manipulate individual pixels in either plane without resorting to read-modify-write access cycles. This provides another twofold improvement in memory bandwidth.

Line Buffer – Within each line of LCD video data, bytes must move from the frame buffer to the scroller/CLUT in an unbroken stream at 48Mhz. Although the frame buffer is capable of burst transfers of 60Mpixels/sec, it cannot be depended on to

maintain that speed for more than one SDRAM page (256 pixels). At page boundaries, the SDRAM must initiate a new page access, and potentially satisfy refresh requirements. Since video lines are longer (640 pixels) than SDRAM pages, some mechanism is required to smooth the flow of pixels from the frame buffer to the LCD.

This smoothing is provided by a 1024 byte dual port line buffer, implemented in a pair of FPGA block RAMs. At the end of each active LCD line, the video timing generator requests a new line of pixels from the frame buffer. The memory arbiter services the request by bursting 640 pixels from the frame buffer to the line buffer, using the video address supplied by the timing controller. The entire line of 640 pixels is moved at maximum memory speed, taking a little over 11µs to complete at 60Mhz. The pixels are then clocked out of the line buffer and presented to the scroller/CLUT at a constant 24Mhz, taking about 30µs per line. Double buffering is not required, as the burst fill rate far exceeds the 24Mhz drain rate, and the fill begins during the generation of horizontal sync, giving the controller plenty of head start on filling the line buffer before the timing generator begins draining them out.

To keep the control logic simple, and minimize SDRAM access overhead, each 640 pixel line is transferred from SDRAM in one transaction. This does hold off the ARM CPU for up to 11µs at a time, but as the ARM CPU does not access the frame buffer often, this is not thought to be an issue.

Fill Engine – The 5500 routinely draws rectangular regions on screen for use in dialog boxes and buttons. When drawn by the CPU, frame buffer bandwidth becomes an issue, as random accesses to the SDRAM buffer are inefficient, and many of them are required to fill large regions of the display. To reduce both CPU and frame buffer loading, the LCD controller provides a simple fill engine which automates the filling of rectangular regions of the frame buffer, and takes advantage of the burst capabilities of the SDRAM.

The fill engine interface is simple, consisting of four boundary registers to define the fill region, and one register to record the fill value, and planes to be filled. The fill engine can fill any value into any rectangular region of the display in either or both planes simultaneously. The bounding values (top, bottom, left, right) define the rectangle to be filled in screen coordinates, with 0,0 at the upper left, and 639,479 at the bottom right. The fill value contains both the dynamic (5) and static (3) pixel bits as well as two plane enable bits.

After loading the boundary control registers, the CPU initiates the fill by writing the requested fill value and plane enable bits to the fill value register. The fill is then queued for the next video frame and the fill engine becomes “busy”.

Fills are implemented synchronous with frame refresh. At the completion of each line buffer fill request from the video timing generator the fill engine checks to see if a fill is underway. If so, the current video line position (from the timing generator) is compared to the top and bottom boundary registers. If the current line is between the top and bottom, the fill engine adds the left boundary value to the current line memory address (as provided by the timing generator) and proceeds to write the fill value into memory until the address matches the right boundary. Depending on the width of the filled rectangle, fill bursts can take anywhere from 100ns to 11µs.

In this way, the fill engine follows the video timing generator down the screen, replacing pixels in the frame buffer immediately after they are sent to the LCD. This synchronous operation makes efficient use of the existing address generation hardware and provides “flicker-free” fills, regardless of region size. If fills were

unsynchronized, they would often cross two successive display frames and result in visible tearing or flicker. As a result of this frame synchronous operation, fills always take one frame time, regardless of their size, and complete coincident with the end of the frame.

Main State Machine – The SDRAM frame buffer is constantly in demand by the CPU, the video timing controller and the fill engine. The CPU manipulates pixels in the frame buffer in real time to construct the visible display while the video timing controller manages the constant stream of pixels from the frame buffer into the line buffer, and on to the scroller/CLUT. At the same time, any requested fills must access the frame buffer to write the requested fill region. When all three contend for access to the frame buffer simultaneously, memory bandwidth can exceed 100Mbytes/sec.

The Main State Machine manages all these competing requests on a priority basis, with display refresh taking top priority, followed by fills and finally CPU accesses. The state machine runs at 60Mhz, processing line buffer fill requests from the video timing generator, fill requests from the fill engine and read/write requests from the CPU. The 5.3 pack/unpack logic and fill engine logic are actually various states of the Main State Machine.

Interrupt Management – The LCD controller produces two interrupts to notify the CPU of the completion of important tasks. At the end of the active region of each display frame, the controller can generate an interrupt to tell the CPU it has uncontested access to the frame buffer for a short period, and to synchronize display related processes in the CPU (such as waveform drawing and scrolling control). A similar interrupt is provided to signal the completion of fills. Both interrupts may be disabled and/or acknowledged in the system control registers.

Video Waveform Scroller

There are numerous ways of achieving a scrolling waveform, none of which is supported by standard LCD controllers. The MAC 5500 provides scrolling through FPGA hardware placed between the LCD controller output and the LCD panel input.

To produce the scrolling effect it is necessary to maintain two virtual image planes, one atop the other. Static (stationary) objects are drawn in the static plane, which appears nearest the viewer and may be either opaque or transparent. Dynamic (scrolling) objects are drawn in the dynamic plane, which appears behind the static plane and is always opaque, though not necessarily visible. The appearance of motion is achieved by continuously changing the start point for display of the dynamic plane from one video frame to the next.

Since the LCD controller does not support multiple image planes, it is necessary to pack two planes of image data into a single frame buffer. On the software side (during drawing) this is done by bit masking operations that allow separate manipulation of two virtual pixels in each byte of frame buffer memory. Each 8-bit byte holds a pair of pixels, one from the static plane and one from the dynamic plane.

On the hardware side, part of each frame buffer byte (the static plane) is played directly into the LCD after suitable color mapping. The remainder of the byte (the dynamic plane) is stored in a 1 line temporal buffer before being displayed. The amount of delay applied to the line buffer before merging it with the static image data determines its placement on the screen. By gradually changing the delay, the dynamic image can be made to scroll.

Color Lookup Table (CLUT)

Generally the dynamic plane is filled with waveforms and perhaps a few characters of text. The static plane often contains text messages, icons, buttons and graphics. The greater variety of object types displayed in the static plane demands a wider range of colors. For this reason, each video data byte is split asymmetrically into five bits of static pixel data and three bits of dynamic pixel data. This has come to be known as 5.3 format.

The 5.3 format provides a palette of 2^3=8 colors for dynamic objects and (2^5)-1=31 colors for static objects (1 of the colors is transparent, leaving 31 real colors). In practice, to "freeze" dynamic objects in the static plane requires that the 8 dynamic colors be replicated in the static color map, leaving only 31-8=23 new colors available for static objects. The FPGA implements a writable color lookup table (CLUT) to map the pixel values to sensible colors on the LCD. The CLUT provides 32- to 24-bit entries, providing access to the complete color space offered by the LCD panel. The color mapped LCD data is also fed to three external discrete 6-bit DAC's to create analog video for an external CRT.

Blank/Sync

External VGA monitors are supported with two styles of video sync signal as well as retrace blanking.

Video Sync – The horizontal and vertical sync pulses from the LCD controller are combined to produce a composite sync signal that is added to the video signal. The video sync signal may be disabled under software control to accommodate monitors that do not accept sync on green. The sync signal is applied to all three video guns to eliminate color shifting in systems that do not perform blank level video clamping.

TTL Sync – For monitors that do not accept sync on green, TTL logic level horizontal and vertical sync signals are provided. These may be enabled/disabled to implement a rudimentary "sleep" operation on Energy Star compliant monitors.

Blank – Unlike LC displays, CRT's emit light from more than just their active display surface. The electron beam is visible even during retrace and precautions must be taken to ensure that the guns are off in non-active areas of the display. To ensure black borders on external monitors (and reset the DC restore clamps in the video output buffers). The CLUT video passes through a gating register before leaving the FPGA. This allows the LCD DE (display enable) signal to force the guns to a blanking level during inactive portions of the display frame.

Interrupt Controller

ATMEL AT91RM9200 supports one external fast interrupt input(FIQ) and seven external interrupt inputs. In addition all the GPIO lines can act as an interrupt inputs. All the dedicated external interrupt inputs are multiplexed with GPIO ports. The FPGA interrupt logic combines the interrupts form System Timer, Acquisition interface, BBUS interface, Thermal printhead interface and LCD controller to FIQ and Slow Interrupt. The FIQ and Slow Interrupt from FPGA Interrupt controller are fed to processor FIQ and IRQ0 respectively. For more detail on the operation of the interrupt mask/status registers, see the source file "hardware.h".

System Interrupt Timer

A 1KHz timer generates system interrupts (which may be routed to FIQ or IRQ) once every millisecond. This interrupt provides the foundation for all operating system timers.

Acquisition Module Interface

Overview

The MAC 5500 acquisition module communication protocol is different from previous generations in several key respects:

1. Acquisition module timing is synchronized to the system.

   There is no longer a need to play synchronizing games to get the system (especially the display and printer) operating at the same sampling rate as the acquisition module.

2. Data is framed and has checksum.

   Previous acquisition modules offered rudimentary error detection. This has finally been done nearly right. Each ECG data packet contains a checksum.

3. Commands do not interrupt the data stream.

   Previous generation acquisition modules required a cessation of sampling to transmit commands to the module. This cessation of sampling had the undesirable effect of breaking the acquisition stream for operations as simple as changing the line filter frequency or enabling or disabling the pace pulse detector. With the MAC 5500 this restriction is removed.

4. Buttons are supported.

   Button state is communicated to the system in each ECG data packet. This allows limited operator interaction with the machine via the acquisition module.

Details

A constant reference clock frequency of 1MHz must be provided to the acquisition module for generation of its internal sampling clocks. To eliminate the need for data lines, command information is encoded on this reference clock by altering its duty cycle. The FPGA provides a serializer for the command bytes and clock generator/ modulator to transmit both the clock and command bits from the serializer. The reference clock duty cycle is nominally 50%. By altering the duty cycle, the DC content of the clock is changed. The acquisition module detects this change in DC level. The timing of these shifts in DC offset encode command data bits. A zero is encoded as a single shift in duty cycle from 50% to 25% lasting 31.25µs, followed by a refractory period of 468.8µs. A one is encoded as a pair of 31.25µs periods of 25% duty cycle separated by 93.75µs, followed by a 343.8µs refractory period. In either case the transmission of a single bit takes 500µs. A higher level protocol organizes commands as groups of 8 bits.

Data from the acquisition module is packed into 257 bit NRZ frames. The receive line idle state is high. The first bit of each packet is a zero and serves as the packet start bit. As with a UART, the start bit is discarded. The following 256 bits are received into a 16-word x 16-bit buffer for use by the ATMEL CPU. The receive logic then looks for an idle period (analogous to a UART stop bit) of at least 125µs in length as an indicator that the link is again idle. Special marker words are inserted into the ECG data packet (words 5, 10 and 15) to guarantee there will never be a run

of more than 80 bits of one's (or zeros for that matter), so there is no possibility of satisfying the idle period requirement in the middle of a data packet.

Because the acquisition module clock is supplied by the FPGA, receive timing errors are limited to phase uncertainty. By searching for the beginning of the start bit in a fashion similar to that used by a UART, the phase uncertainty is eliminated and the remainder of the packet may be received without further synchronization. In practice, the FPGA uses every edge in the receive data stream to re-sync its bit sampling circuit. It is possible for the ECG data to be all zeros or ones, so runs of as many as 80 zeros or ones could occur before a marker word is encountered in the data stream (which contains at least one "1" and one "0" to break any runs in the data).

The acquisition module supports a special "code update" mode for rapid reprogramming of its on-board code memory. To increase the update speed, the acquisition module echoes each uploaded code byte with a single reply word rather than the usual 16-word data packet. The FPGA receive logic provides a special 1 word reception mode to accommodate this.

Thermal Printhead Interface

The ATMEL CPU sends print data to the thermal print head through a buffered serial interface. The FPGA implements the data buffer, serializer, strobe/latch pulse generator and power switch gate drive pump. Special interlocks are implemented to prevent stuck strobe signals or printing when the battery voltage is critically low.

Each print line requires 1728 bits of data. To conserve FPGA resources, each line is divided into three chunks of 512 bits each, with one leftover chunk of 192 bits. The FPGA provides a single 32 word x 16 bit buffer (512 bits) to hold the print line data. After writing a chunk of data to the buffer, the ATMEL CPU enables serialization of the data by reading one of two registers (to support the serialization of either a full 512 bit or partial 192-bit buffer). When the entire print line has been loaded, the ATMEL CPU cues a print strobe by writing the required strobe width value to the strobe/latch pulse generator.

When the strobe register contains a non-zero value, the power switch gate pump produces a differential clock signal to drive an external diode voltage doubler (CR132-133, C262-C264, R291). The output of the voltage doubler drives the gate of a power MOSFET (Q11) that provides power to the print head. R289 provides gate bleed off to ensure that Q11 turns off when the pump stops. C279 filters the doubler output to DC.

A special test mode is provided to allow testing of the thermal print head. In test mode, print head power is disabled and the strobe signal is driven continuously. This allows individual print dots to be driven with a small test current via a current source (Q107, R322, Z100) enabled by a level shifter (Q106, R321) driven from a ATMEL GPIO line. Half of the resulting printhead voltage drop (divider R323/324) may be measured to either determine the dot's resistance or at least determine if the dot is open.

Serial EEPROM Interface

A standard four-wire SPI interface is provided for connection to a serial EEPROM memory (CFGMEM). The ATMEL exchanges a byte of data with the EEPROM by writing a value to the interface register. Data is clocked at 4MHz; quickly enough

that no interrupt support is required. The ATMEL CPU polls a ready bit to determine when the transfer is complete.

BBus Interface

There are several I/O functions poorly suited to direct control by the ATEML CPU, whether for reasons of software complexity or power consumption. These I/O functions are provided by three 68HC705 microcontrollers placed strategically around the board (Moe, Larry and Shemp). Each of these three microcontrollers must communicate with the ATMEL CPU. BBus is a simple 1-wire point-to-point interface designed specifically for this purpose. The FPGA provides a single BBus transceiver and a 3-way bidirectional multiplexer to attach the three BBus microcontrollers. For more Bbus information see the microcontroller firmware source files. From the programmer's standpoint, BBus operates like SPI, where each transaction exchanges a single byte between the host and peripheral.

PWM Analog Outputs

Four PWM channels are provided for the generation of analog outputs. Three of the outputs are available on the Analog I/O connector; the fourth is available internally for future use (if any). One of the PWM channels provides 12-bit resolution at 6KHz cycle rate; the other three provide 8-bit resolution at 96KHz cycle rate. The ATMEL CPU simply writes the desired value into a PWM data register and the output duty cycle changes on the next PWM cycle. External analog circuitry converts the PWM logic signals to smooth analog voltages. The 12-bit PWM channel is intended for ECG output and produces a swing of +10 to -10V. The two 8-bit channels provide a unipolar 10V output. Regardless of the resolution or swing range of each PWM channel, the FPGA treats the data value as a signed 16-bit number representing a voltage from +10V (0x7fff) to -10V(0x8000). Logic in each PWM channel ensures that the closest possible voltage is generated for each data value (ex. 0x8000 on an 8-bit channel produces zero volts output).

The FPGA PWM output signals contain a substantial amount of noise from +3V-M supply fluctuations. To reduce noise and establish an accurate reference level, the PWM signals are buffered by CMOS inverters (U20) that are powered from REF2V5. Although the CMOS inverters are powered by 2.5 Volts but are driven by 3.3 Volt logic, no problem exists as this is allowed with VHC logic. The PWM output signals are then low pass filtered (R186,C186, etc) before being passed to the output amplifiers. The ECG output channel amplifier injects an offset current derived from REF2V5 to achieve bipolar operation. The DC outputs operate in unipolar fashion, eliminating the vexing MAX-1 offset problems. No zero calibration is required for the DC outputs. Since the ECG output is an AC signal, no offset adjust is required there either.

The output amplifiers provide additional low pass filtering (R178,C178, etc.). ESD protection and additional PWM carrier filtering is provided by 0.1µF filter capacitors. To prevent amplifier oscillation, blocking resistors are placed between the amplifier outputs and the filter capacitors.

Beep Generator

A simple tone generator with two volume levels provides system beeps and key clicks. Frequencies of 250Hz, 500Hz and 1KHz are provided at both low and high volume. The logic level output signal drives LS1 through an open collector

transistor driver Q100. Full volume is achieved by driving the fundamental beep tone directly to the speaker. Half volume is achieved by gating the speaker signal with a 48KHz square wave, reducing the amplitude by 50%. The LS1 is also used by the communication board for modem sound. The modem speaker signal from the module is amplified and driven though Q101.

PC Card Logic

The -006 and -007 board is designed to support multiple products and one of the requirement during the design phase was the support for PC Card, through a daughter board. But this requirement was removed later on. The PC Card logic use the two ATMEL chip select signals and bus control signals to generate, IO, Memory and Attribute memory access to PC Card. The PC Card bus controls signals from FPGA and the address and data lines form ATMEL are buffered and terminated to daughter board interface connector J21.

SDRAM

Program code and working data is stored in a four 4MWord bank of 32-bit wide memory (64Mbytes). This memory is made up of two 256 Mbit SDRAMs each 16 bits wide. All bus timing and refresh control is performed by the ATMEL CPU SDRAM controller. The SDRAM clock rate is one third of the ATMEL CPU clock or 59.904 Mhz. Though the size requirement is less, the video frame buffer also use 256Mbit SDRAM.

NAND Flash

There are two 32 Mbytes NAND Flash in -006 and -007 boards. One is used for storing FPGA configuration data and system software. The other is for data storage. The access to NAND flash is through a dedicated smart media interface logic provided by ATMEL CPU. Unlike the -005 board, NAND flash chips are accessed through the buffer U55 instead of Xbus. The NAND Flash control signals are changed to GPIO mode while configuring FPGA in fly by fashion. Wear-leveling algorithm is implemented for the data storage NAND flash to extend the life.

Secure Digital Card Interface

The SD card interface is provided to support software update and external data storage application. The socket provide card detection and write protect status signal. ATMEL CPU has built in secure digital card interface controller. But there is a bug in the current revision of the ATMEL CPU, which swaps bits within the transmitted / received nibbles. Since the software overhead to correct this is high, SD card interface support only SPI mode. However all the SD card interface signals are terminated at the connector through a set of resistors, which are not placed, so that we can go for the true SD card interface in future.

Serial EEPROM

System setup information, option enables and other machine specific data is stored in 32 KByte serial EEPROM. The SPI interface to the EEPROM is provided by the FPGA.

Daughter Board Interface

The interface is realized using a 100 pin high speed connector. This interface provide two serial interfaces, PC Card interface signals, USB host and various power supply tappings. The PC Card interface and USB interface are no longer in the requirement list. All the PC Card signals are buffered. The buffer will be active only when a valid PC card is inserted in the daughter board. Out of the two serial interfaces, one provides full hardware handshaking. This is derived from the Super IO COM2. The COM2 can be routed to either COM2 external connector or to the daughter board interface using a multiplexer controlled using ATMEL CPU port pins. The second serial interface has limited hardware control and derived from ATMEL CPU UART 1.

VGA LCD/CRT Interface

An internal backlit LCD is home for the MAC 5500's graphical interface. In addition, external VGA monitors are supported for stress applications. Control for a standard VGA format (640 x 480 pixels) LC display is provided by the FPGA. The board is designed to support MAC3500 LCD display also. Though the interface to LCD is same, external CCFL backlit inverter is different for both display. Two connectors are provided for external CCFL backlight inverters as well as two digital controls for On/Off and brightness. While the FPGA is capable of directly driving the LCD, external hardware is required to generate the analog video levels expected by external VGA monitors.

LCD Panel EMI Reduction Components

To reduce EMI, 47pF capacitors have been added to all LCD digital lines. In addition, 49.9Ω resistors have been added to the video clock and Sync lines.

CRT Video DAC / Sync / Buffers

A triple 6-bit video DAC supports external analog VGA monitors. Only one DAC/ Level Shifter/Buffer will be described, as they are all identical in function. The video output is referenced to a filtered tap (FB107, C29) off the +3V-M supply rail and then level shifted back to ground.

Each DAC is comprised of six binary weighted resistors and a seventh blank/sync signal resistor. The FPGA LCD data outputs sink current through the 75Ω load resistor in proportion to their respective DAC resistors. The voltage across the 75Ω load resistor represents the sum of all drive currents. Minor non-linearity is introduced in the DAC transfer function by the fact that the summing junction varies in voltage with DAC current.

The 3.3V referred video is shifted back to ground by a blocking capacitor. The shifted video signal is buffered (and further shifted) by emitter followers. Transistors clamp the negative excursions of the bases of the emitter followers to one diode drop above ground, so the most negative level at the emitter of the emitter followers is ground. Nominal full-scale swing is 1VP-P (blank to white).

Bias for the base of the clamp transistors is provided by a 1.4V bias supply consisting of a stack of two diode connected transistors (Q8). This 2Vbe bias exactly cancels the 2Vbe shift produced by the level clamp and output buffer. Since all

transistors are of the same type their Vbe's track well enough to provide acceptable output offset.

Diode clamps to ground and +3V-EMI provide ESD protection for the VGA video and sync signals. The +3V-EMI rail is isolated from ESD transients by FB106.

Acquisition Module Transceiver / Power Switch

MAC 5500 acquires ECG data with a new generation CAM acquisition module. The FPGA provides the interface logic. Clocks and commands are transmitted to the acquisition module on a balanced RS485 line. Data is received similarly. Power to the acquisition module is provided by a software controlled linear regulator.

Transceiver

To reduce EMI and susceptibility to noise, the acquisition module link is implemented using RS-485 differential signaling. An RS485 interface device provides the single ended to differential conversion in both directions. Ferrite beads, capacitors and resistors are used to reduce EMI on both sides of the transceiver.

Acquisition Power Regulator / Switch

To reduce standby power consumption, acquisition module power is switchable. To protect the acquisition module from temporary brownouts on the main 12V supply, power is obtained from a parasitic winding on the main 5V regulator. This voltage is not well regulated, so a linear regulator (U18) is used to provide regulation. This regulator also sports an enable input which is used to disable power to the acquisition module when not in use. The regulator also has build in current limit and over temperature shutdown for protection.

COMM Port Power Switch / Current Limiter / KISS Power

Power for external peripherals such as a modem or the KISS vacuum electrode pump is available on the COMM connectors. Power may be turned on/off under software control and current limiting is employed to protect internal operations from excessive external loads. The current requirements and startup conditions of the KISS pump require very high currents. U.L. limits power to external devices to 15 Watts for reducing the likelihood of fire during overload. The KISS and U.L. requirements conflict to a degree that a simple current limiter will not satisfy both needs therefore a special current limiter circuit had to be devised. Six Sigma project #27118 Mac3000 Com Port Power Circuit project addressed this issue and is implemented in this design.

Since currents exceed 1 Ampere and the supply is 12 Volts a linear current regulator is impractical since the pass element would need a heatsink. The method chosen here was to use a FET (Q2) as a switch (a switch is either on or off and in both cases dissipates little power). In normal operation the ENIOPWR signal is driven high by software to activate the power switch. This signal saturates transistor Q103 which provides the gate drive for the dual FET Q2. Both P channel FETs of Q2 are used and therefore are connected in parallel. Return current from the load is sensed by shunt resistor R6 (0.1Ω). U9 is used as a differential amplifier to boost this current sensed signal. U7 is used as an integrator which integrates the amplifier current limit signal before entering comparator U8. When the current exceeds the comparator

threshold the open drain output of the comparator is used to remove the gate drive from Q103 which will in turn switch off the com port power. The function of the integrator is two fold. First it allows high surge currents to exist for a short time. Secondly the integrator has a much longer recovery time due to diode CR103 which effectively changes the integration resistor from 100KΩ to 1MegΩ. This long recovery time results in a low duty cycle when the load is a short circuit. The low duty cycle prevents FET Q2 from overheating when driving a short circuit.

Since the MAC 3500 contains an internal KISS pump, separate power control is necessary for this CPU board design to support that product. An identical Switch / Current Limiter circuit as described above for the COMM Port Power was added exclusively for the KISS pump.

Thermal Printhead Power / Pixel Test Hardware

The FPGA provides all the interface logic for the thermal print head. A MOSFET switch controls power. A charge pump voltage doubler driven by the FPGA provides that switch's gate drive.

Additional circuitry (currently unsupported) is supplied to allow the measurement of individual dot resistance for automatic strobe width compensation and blown dot detection. A switchable constant current source (6mA) applies a test current to the TPH power bus. Larry then measures the TPH power bus voltage (one of the four analog inputs he continuously monitors). By loading a single black dot into the print head it is possible to measure its resistance. A typical TPH has an average dot resistance of 650Ω. Presuming negligible driver leakage current, a single enabled dot would drop 3.9V. While there are mitigating influences (off-pixel driver leakage current and on-pixel driver saturation voltage) that might make accurate pixel resistance measurements difficult, it is certainly possible to differentiate pixels of nominal resistance from those that are blown open.

Super I/O Peripheral Controller

A PC standard Super I/O peripheral controller provides two serial channels (one IrDA compatible, and a clock/calendar.

RS-232 Serial Ports (One Dual Mode RS-232 / IrDA)

Four serial ports are provided on two back panel Mini-DIN 8 pin connectors. The Super I/O device provides two serial ports (COM1 and COM2) and two more (COM3 and COM4) are provided by the ATMEL CPU. The COM2 serial port and modem handshake lines are found in the COM2 connector. COM1, COM3, and COM4 serial ports use pins in the COM1 connector. The COM2 serial port of the Super I/O device also supports the IrDA interface. The COM1 serial port from Super I/O is multiplexed with serial debug port of ATMEL. The multiplexer select pins are controller by the jumper(W2) setting. Other than the above mentioned COM ports, an additional com port, COM5 is provided by ATMEL. This is terminated to daughter board interface connector and is used by the communication board Ethernet module.

RS-232 level shifting is provided by two transceivers. Each produces the necessary drive voltages with internal charge pumps. The devices are rated to withstand ESD

onslaught, so no external ESD protection is provided. The transceivers may be shut down under software control to conserve power.

Clock/Calendar

The Super I/O device provides a clock /calendar function. Backup battery power is provided by a “super” capacitor (C21) with sufficient storage capacity to power the clock for hours after main battery removal. This backup source provides sufficient time to exchange battery packs when necessary. Diode CR106 charges C21 when the main system power is up. R179 limits the charging current to a safe level.

PS2 Keyboard Port

External card / bar code readers may be connected to the MAC 5500 via a PS-2 compatible keyboard port. A small amount of 5V power is available at the connector to power the external device. Power faults are detectable. EMI and ESD protection are provided.

The Three Stooges

System management and some low level I/O functions are implemented in preprogrammed 68HC05 microcontrollers. Moving some I/O functions out into small processors relieves the ATMEL CPU of burdensome real-time chores and moves the control hardware closer to the controlled devices, potentially reducing EMI. Localizing control also promotes reuse in future designs as the functions are self contained and reasonably portable.

Originally there were four Stooges. Since the boot loading and FPGA configuration is handled by ATMEL CPU, the Curly was removed in -006 board. Although there are three of these little fellows in the MAC 5500, each performing a different function, there is only one firmware image. By merging the code from each of the three functions into a single ROM image, cost and confusion are reduced. It is impossible to place a processor in the wrong spot on the board and a single pile of paperwork supports all of the MAC 5500’s 68HC05 production volume. More detailed information may be found in the source code.

Startup Self Identification

As each controller is released from reset, it executes a common “WhoAmI” routine to determine its identity on the board. Each controller’s environment is uniquely and easily identified with a few port pin tests. Once the identity is discovered, the code jumps to the appropriate entry point in the unified image and microcontroller assumes the desired personality.

The flow for the “WhoAmI” routine is as follows:

- **Run ChkMoe:** Basically if the BBus (PD5) is low we are Moe. Since Moe controls the power supply for +3V-M which is off at the moment, the BBus pull-up resistors will actually pull the BBus lines low. This can only occur with Moe since all other Stooges are powered by +3V-M, Moe is powered by +3V-C instead.
- **Run ChkCurly:** Though the Curly is removed, the firmware related to Curly is still present, for backward compatibility.

- **Run ChkShemp:** If bit 4 of Port A is high, we are Shemp. At this point we are either Shemp or Larry. Shemp has pull-up resistors on Port A so bit 4 should be high. Larry on the other hand has uses Port A to drive a makeshift DAC. Since Port A is not being driven at the moment, bit 4 will be pulled to low via the common DAC resistor R315, which is grounded.
- **We must be Larry.** At this point we have eliminated all other Stooges.

BBus

All three stooges (Moe, Larry and Shemp) communicate with the ATMEL CPU via BBus connections. BBus is a single wire, half-duplex serial connection that places minimal hardware requirements on the microcontroller while yielding respectable bit transfer rates (~50KBps). A common set of BBus commands allow the ATMEL CPU to access 128 bytes of RAM in each microcontroller. This dual port access allows the ATMEL CPU to examine and modify internal variables in each controller while code is executing. This ability is used to allow the unalterable HC05 code to handle modest changes in hardware, such as changes in paper drive gearing or battery pack capacity.

Shemp

Similar in function to the ABus keyboard controller in Max-1 architecture machines, Shemp scans the keyboard and queues key presses for the ATMEL CPU. Unlike previous designs, key presses are reported both on press and release, allowing system software to implement auto-repeat as well as the continuous operation of treadmill control keys (up/down, faster/slower). A special key code indicates when all keys are up as a safeguard against stuck keys in the application software.

Unlike previous keyboard encoder designs, Shemp does not provide dedicated scan hardware for the shift and / or option keys. These keys are now located in the scan matrix. Careful placement of keys in the scan matrix allows simultaneous depression of the shift, option and other keys without interference.

Larry

Larry controls the paper drive motor and digitizes the analog inputs. The motor control functions are virtually identical to those offered by the 78310 processor in Max-1 architecture machines, with an expanded speed control range (down to zero). Since Larry's code is not field-alterable, every motor control parameter is alterable via BBus. Hopefully this renders the code immune to minor changes in the printer drive train.

Motor Speed Control

Larry controls the motor speed by delivering a DAC controlled drive voltage to the motor windings. The 6-bit DAC is implemented using discrete, binary-weighted resistors directly driven by Larry's port pins. The DAC output voltage (approximately 300mV full scale) is compared to a filtered fraction of the applied DC motor voltage by comparator U61. If the motor feedback voltage is below the DAC voltage, the comparator turns on the motor via an H-Bridge driver. One motor terminal (which one is a function of motor direction) is always grounded. The other is alternately driven to either 12V or ground. The duty cycle of the drive signal determines the average applied voltage and therefore the average motor speed. The feedback voltage signal is the average of both motor terminals (R274 and R275

driving R312), with a 50:1 ratio, 15Vin = 300mV out, hence 15V full scale). Since one terminal is always zero (grounded) and the other is driven with a variable duty cycle between zero and 12V, the feedback signal is positive regardless of motor direction. C259 filters the switching noise from feedback voltage.

NOTE

The frequency and duty cycle of the motor drive signal are random. This serves to reduce EMI by spreading any emitted noise across a wide frequency spectrum. An RC snubber (R273 and C260) suppresses ringing on the motor lines.

Larry maintains precise motor speed control by comparing the frequency of the tachometer pulse train emitted by the motor's integral encoder to an internally generated reference frequency derived from Larry's resonator. Larry processes motor position information on both edges of both encoder signals for a total of 64 loop correction cycles per rotation of the motor shaft. This high angular sampling rate allows Larry to achieve accurate and smooth speed regulation down to zero speed.

Paper Jam / Pull Detection

Larry monitors the servo error variable to determine whether the servo loop is closed. If the error variable saturates “on” for more than a predetermined time it is assumed that the paper drive torque has become excessive, or the motor has stalled. This condition is reported as a *Paper Jam Error*.

Similarly, if the servo error variable saturates at “off” for more than a predetermined time, it is assumed that the someone is pulling on the paper with a force that exceeds the paper drive system torque, and as a result paper speed has been pulled out of regulation. This condition is reported as a *Paper Pull Error*.

Cue Hole Sensor

Cue and out-of-paper conditions are sensed via the thermal print head's integral optical cue sensor. Larry monitors the cue sensor’s logic output.

Cue Hole Detection

Larry monitors the output of the cue sensor to detect the presence or absence of paper under the sensor, and hence the absence or presence of cue holes.

Paper Tracking Fault Detection

Larry monitors the cue sensor for abnormally long paper travel without encountering a cue hole. This condition is reported as a *Paper Fault*.

Paper Out Detection

Larry reports excessive paper travel without sensing paper as a paper out condition.

Analog Inputs

Larry digitizes four analog inputs at eight bits resolution each. Two inputs handle external analog signals, such as those produced by ergometers or analog output blood pressure monitors. Thermal printhead temperature is measured for use in compensating strobe pulse width to maintain constant print density over a wide range of thermal printhead temperatures. The output of the thermal printhead pixel test hardware is also digitized to allow the resistance measurements on individual print elements.

Moe

Moe is responsible for controlling and monitoring the battery, power supplies, on/off key, system reset and related functions. Moe runs continuously from +3V-C, even in the absence of AC power. This continuous operation is necessary for Moe to accurately monitor the battery state of charge and detect power key presses.

System Startup

When the system is off and the user presses the power key, Moe begins the startup sequence. If the battery contains sufficient charge, or if AC power is applied, the main CPU board power supplies (+3V-M and +5V-M) are enabled and after a suitable stabilization period SYSRESET* is released. Moe then keeps tabs on the system via a software watchdog that must be serviced by specific BBus activity from the ATMEL CPU. Moe himself is monitored by a self contained MAX823 watchdog timer / brownout detector. Moe must constantly toggle the MAX823 watchdog input pin or suffer the consequences.

NOTE

Moe presumes that the main power rails, which it controls, are off when it powers up. If Moe should malfunction while the system is already powered it is likely that the HC05 will incorrectly identify itself as Larry. Larry's default power-up state results in its port pins assuming a state that disables +3V-M. Since Larry does not service the watchdog chip (WDOG), another reset will follow within 2 seconds. As +3V-M is now down, Moe will be selected at the next restart.

When SYSRESET* is released, ATMEL CPU configures the FPGA and load secondary boot program from information stored in NAND Flash. Moe expects the ATMEL CPU to request status via the BBus interface after startup. If that request doesn't arrive in time, Moe places the system back in reset and removes power. The time is set as two minutes six seconds for this version. This time-out considers the time for software update. There is a provision to disable the Moe watch dog monitor using jumper W1. This is to facilitate the debug tool connectivity.

In the event of main CPU failure that causes loss of function yet maintains Moe's watchdog function, a manual forced power-down function is provided. A continuous press of the power key for a period greater than 5 seconds will force the system to shutdown.

AC Power/Battery/Charger

Battery and system power management is entirely Moe's responsibility.

An off-the-shelf 28V 1A universal input power supply provides operating/charging power for the MAC 5500. Located in the bottom of the chassis, the power supply is disconnected from the CPU board when the lid is open. The battery connection is maintained through the hinge so the CPU board is capable of operating for a limited time with the door open.

An LT1511 switchmode charge controller (Battery Charger) provides battery charge current. This device monitors both battery and power supply current draw and maintains both at safe levels. As system current draw increases, the Battery Charger automatically decreases battery charging current to maintain total power supply current below the design level (nominally 1A). Nominal charge current is also 1A, which is achievable only when the system is off.

Moe enables / disables the charger via CR102. When Moe pulls the CHRGTRL line low, CR102 sinks current from the Battery Charger's VC pin shutting down the error amplifier and disabling switching. R119 ensures that the charger remains off when Moe is starting up.

Lid Open Detection

A self-aligning connector routes power and motor signals from the power supply compartment to the CPU board. When the lid is closed the DOOROPEN signal is shorted to ground. When the lid is open a pull-up resistor ensures a high level on DOOROPEN. Moe monitors this line to detect lid open conditions that are reported to the system software to avoid misinterpretation of motor fault indications. When the door is open, the motor connections are lost and Larry receives no tachometer feedback from the motor. Without knowing the cause of the lost tachometer info, Larry can only respond with a paper jam condition. Moe's knowledge of the lid state is used to suppress this error message as well as prevent further print operations.

AC Power Monitor

Moe senses the presence of AC power through a voltage divider (R102, R103) which drives the under-voltage detection comparator in the Battery Charger (Vtrip = approximately 7V). The battery charger will not be enabled unless the DC power supply voltage is above approximately 21V.

Battery Pack

The MAC 5500 uses a 15-cell nickel metal hydride (NiMH) battery pack with integral thermal sensor for charge termination detection and self-resetting thermal fuse for short circuit protection. Charge current and normal system operating power are obtained from the AC power supply. The charger circuitry monitors both battery charge current and power supply output current. The battery is always charged at the maximum rate possible but system power demands take precedence over charger demands. The charger automatically reduces charge current as required to keep the AC power supply output current within specified limits. In the extreme (during printing) charging ceases and energy is taken from the battery to meet peak system demands. When system power draw declines, all excess power supply capacity is once again delivered to the battery.

Battery Temperature Sensor

Moe uses a thermal sensor inside the battery pack to determine when to terminate charge. During normal charge, the electrical energy obtained from the power supply is stored in chemical reactions in the battery. When the battery reaches full charge there are no more reactants available in which to store chemical energy and the supplied charge power is converted directly to heat. The sudden rise in pack temperature caused by this release of heat is an indicator of full charge. When the rate of pack temperature rise exceeds a certain threshold, charge is terminated. This is the only normal charge termination mechanism. Fully drained battery may give higher temperature rise for initial few minutes. To avoid the premature termination of charge, the threshold is set at a higher level for first five minutes. Abnormal conditions such as battery or ambient temperatures beyond spec, or excessive pack voltage, may also terminate charge. Once fully charged, the battery is maintained by low duty cycle charge current pulses.

Absurdly low voltage readings from the battery temperature sensor indicate an open thermistor. This is used as an indication that no battery pack is present.

The sole purpose for resistor R151 is to protect Moe's ADC (AN3) pin in the case where the temperature signal TBATTERY becomes inadvertently tied to VBATT+. This can easily occur since the two pins are adjacent. Should the short occur, resistor R151 will limit the current and Moe's internal protection diodes will clamp the voltage to +3V-C.

Battery Voltage Sensing

Moe continuously monitors battery voltage during operation. Excessively high pack voltages during charge will cause charge termination. If battery pack voltage falls below a predetermined threshold during operation, the battery gauge is immediately cleared to zero and the main CPU is notified of the critically low voltage. System software then initiates an orderly shutdown to protect the battery pack and prevent loss of date/time.

Ambient Temperature Sensor

Extreme ambient temperatures are not favorable for battery charging. Rapid changes in ambient temperature can cause premature or delayed charge termination by altering the pack's temperature. Moe monitors ambient temperature via the thermistor RT1 to ensure that charging occurs only within the "safe" temperature range as well as to minimize the effects of changing ambient temperature on charge termination (particularly to avoid premature termination, which would give a false "full" reading on the gas gauge).

The battery and ambient thermistors are the same type and value to ensure reasonable tracking. Capacitors C155 and C156 filter noise from the temperature sense lines.

Thermistor Bias Switch

To reduce quiescent power consumption when the system is turned off, a switch disables bias current to the battery and ambient thermistors. Q104, under control of MOE, switches the low side of the thermistor bias networks.

Charge Light

Moe provides power to the amber charge light in the power supply compartment. Moe communicates the current battery/charger state via this light. Four conditions may be indicated:

1. Battery charged (light is off)
2. Battery needs charge (light blinks twice per second)
3. Battery is critically low (light blinks once per second)
4. Battery is charging (light on continuously)

NOTE

If the battery is so completely discharged that the MAX782 VL output (+5V) falls out of regulation, the charge light will remain off.

The charge LED is contained in the power supply compartment and is disconnected from the CPU board when the cover is open. When the cover is closed electrical connections are re-established through the self-aligning connector. As the connections are made in random order, there is a possibility that the VPS and XChargeLED drive lines can connect before the power supply ground. This places a high potential across the LED drive circuit as the power supply attempts to return its output current through the LED. To prevent damage to the LED and driver, it is implemented as a constant current source with a large compliance voltage. Q108

provides the constant current drive, and derives LED operating power from the MAX782 (U27) VL output rather than from +3V-C. Q109 level shifts Moe’s output to the level required to turn off Q108 during off periods.

Software update status

Moe also uses the charge LED for indicating the software update progress indicator. After system power ON, if Moe does not find a Bbus status request within six seconds, it flashes charge LED at 1Hz rate with 50% duty cycle for two minutes.

Battery Gauge

Current flow into and out of the battery pack is monitored by Moe via a pair of INA138s acting as Battery Current Monitor. By integrating the current flow, Moe is able to maintain a reasonable estimate of the battery pack’s state of charge. Moe's A/D converter hasn't sufficient dynamic range to cover the full range of system currents at high resolution so some compromises must be made. The current monitor's full-scale range is set to a value that is likely to encompass normal operating currents. Peaks above this level (6Amps) are clipped. The effects of this clipping are minimal as such high density printing occurs for short periods of time and represents only a small portion of system energy consumption. Quantization error limits the ability to measure the small current that flows when the system is off. To compensate for this, Moe presumes a small constant quiescent current flow from the battery. This flow serves to drain the gauge at a rate estimated to mimic the self-discharge and system quiescent current draws.

Current monitor gain is set by R127 and is nominally 1.8A/V for a full-scale (3.3V) current of 6Amps. A low pass filter (R128 and C134) provides filtering to remove switching noise from the signal.

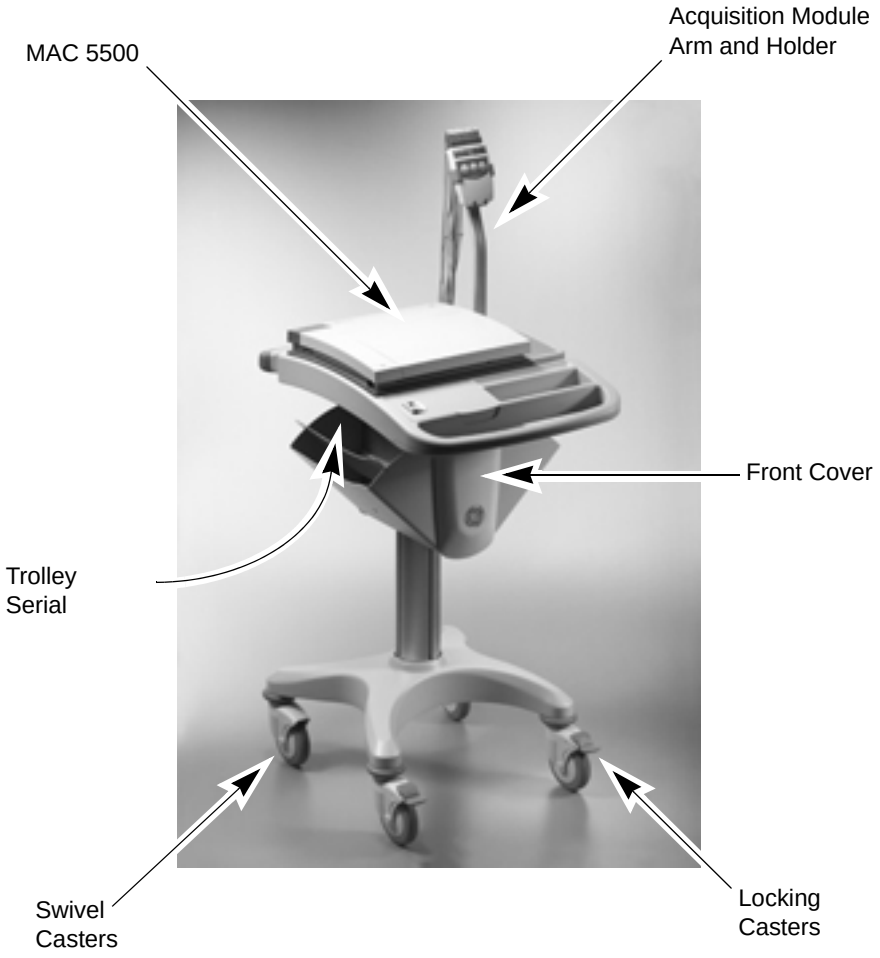
3 Installation

For your notes

Preparation for Use

General

Shown below is a completely assembled optional MAC 5500 Trolley. Use this picture for reference when installing trolley options.



13A

NOTE

Because the optional Trolley is made by another vendor for GE Medical Systems *Information Technologies*, the serial number format is different from that shown in Chapter 1.

Trolley Height Adjustment

The optional MAC 5500 Trolley can be assembled for one of two heights, 92.07 cm (36.25 inches) or 84.45 cm (33.25 inches). The trolley is normally shipped at the 92.07 cm (36.25 inches) height but can be changed to fit your needs. To change to the lower height, use the following steps:

1. Tip the trolley on its side and using a 1/2-inch socket, remove the 4 outer 1/2-inch bolts and slide the base assemble up on the column.

14A

2. Remove the remaining bolts and mounting plate.

15A

3. Flip the mounting plate and reverse the procedure.

CAUTION

Do not over tighten. Over tightening the bolts may cause them to strip.

16A

17A

Installing the MAC™ 5500 resting ECG analysis system

To secure the MAC 5500 to the trolley assembly, follow these steps:

1. Lock the wheels to prevent the trolley from rolling.

18A

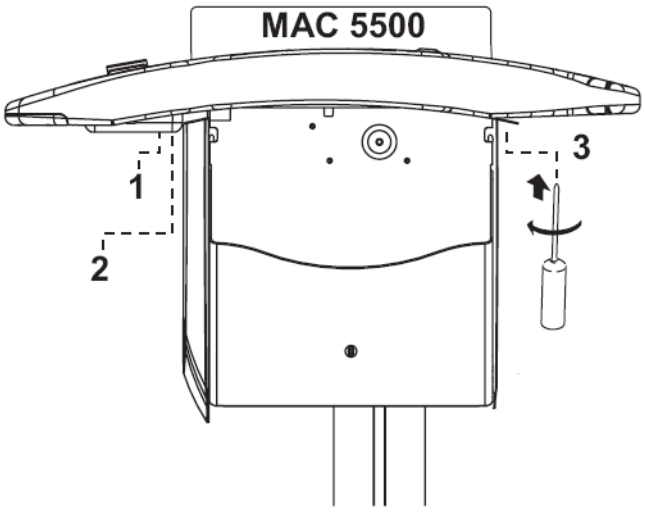
2. Remove the end panel by pulling out and up.

19A

3. Place the unit on the trolley surface, then slide it on until the unit is firmly in place and under the tab at the rear of the on the tray.

20A

4. Secure the MAC 5500 to the trolley by tightening the three captive screws located under the trolley tray.



21A

5. Replace the end panel by pushing up and in until you hear a snap.

22A

6. Unlock the wheels to allow free movement of the trolley.

23A

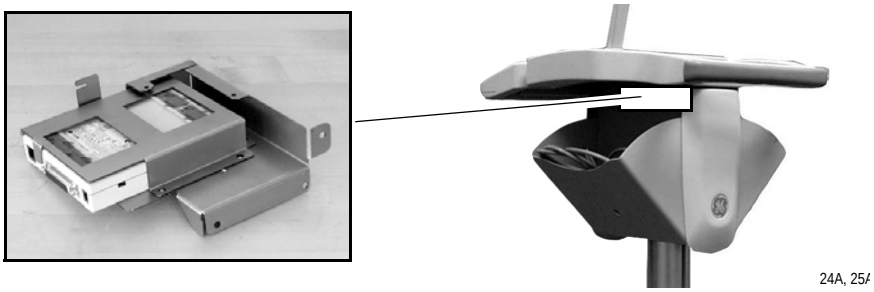
Installing the Optional External Modem Kit

NOTE

The internal modem is standard for the MAC 5500.

The modem and its mounting bracket comes assembled and ready to install on the trolley. To install a modem kit on the trolley, complete the following steps:

1. Find the modem mounting site located under the Acquisition Module support arm at the rear of the trolley where the kit is to be installed.



24A, 25A

2. Slide the assembly up in place so that the bracket slot catches on the bracket lip.

26A

3. Tighten the three mounting screws to secure the modem to the trolley.

29A

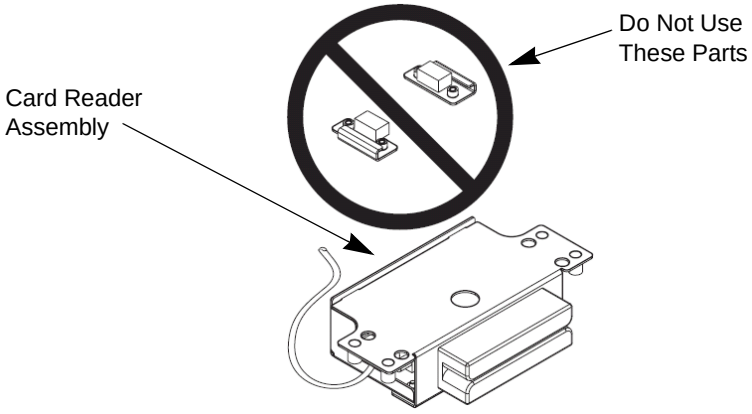
4. Plug the modem cable into connector port **2** on the MAC 5500.

30A

5. Refer to the operator's manual for information on using the modem.

Magnetic Card Reader Installation

The Magnetic Card Reader and its mounting bracket are assembled and ready to install on the trolley. Parts are included for two different trolley styles. Disregard and do not use the parts indicated in the following illustration.



31A

To install the Magnetic Card Reader and its mounting bracket on the trolley, complete the following steps:

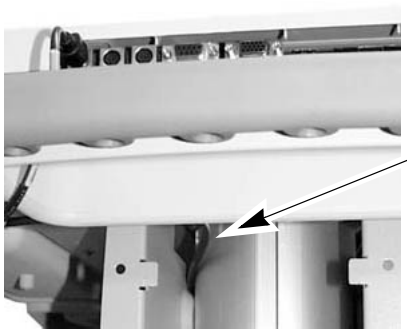
1. Remove both end panels by pulling out and up at the bottom.

19A

2. Using a Phillips screw driver, fasten the card reader assembly under the front handle. Align with holes provided under front handle.

33A

3. Route the cable around the trolley column towards the rear as shown below.



34A

4. At the front, hold the cable to the side so it clears the front panel as you replace the panel.

77A

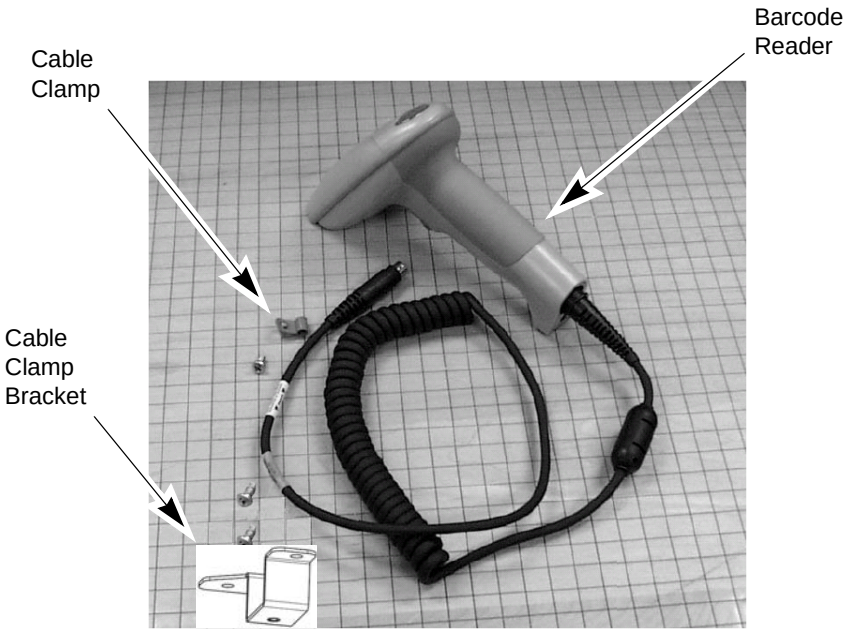
5. Plug the cable connector into port **A** then replace the back panel.

70A

6. Refer to the MAC 5500 Operator's Manual for information on using the Magnetic Card Reader.

Bar Code Reader Installation

The Bar Code Reader and its mounting bracket are ready to install on the trolley. To install the Bar Code Reader and its cable mounting bracket on the trolley, complete the following steps:

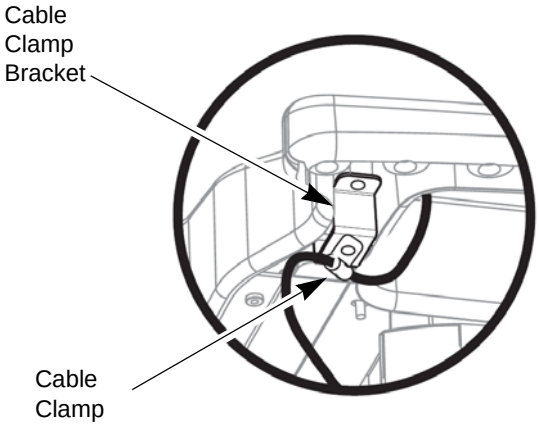


71A, 72A

1. Fasten the cable clamp bracket to the underside of the rear handle using a Phillips screw driver and the self tapping screws provided.

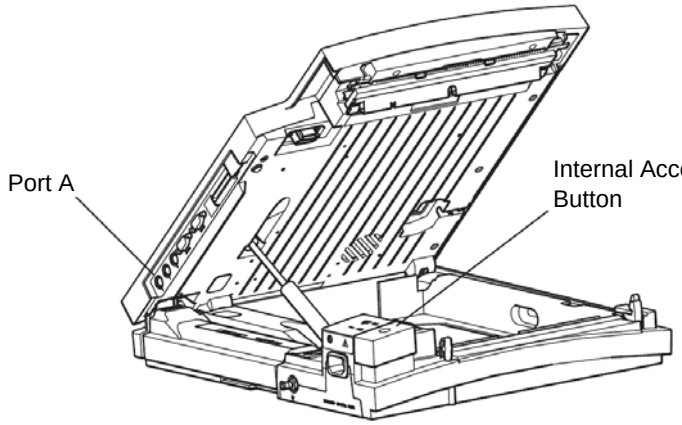
   NOTE

   DO NOT overtighten. Overtightening the screw may cause the screw to strip and clamp to fail.



73A

2. Press the Internal Access Button to open the MAC 5500, then plug the cable connector into port **A.** Opening the MAC 5500 before attaching the cable clamp allows you to place the correct amount of slack to free the cable from stress when the MAC 5500 needs to be re-opened.



3. Next fasten the cable and clamp to the clamp bracket, then close the MAC 5500. Observe that there is enough slack to allow free movement of the cable when re-opening the MAC 5500.

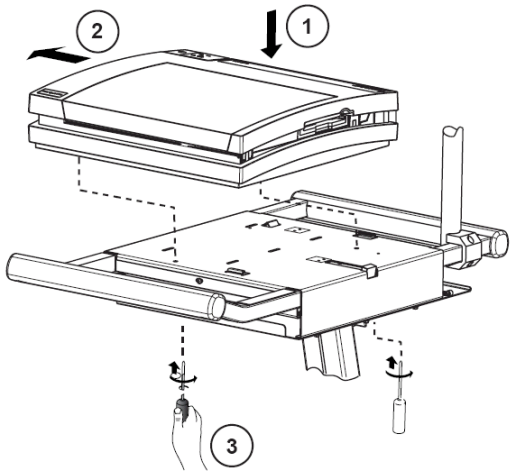
Correct amount of cable slack.

Not enough cable slack.

4. Refer to the MAC 5500 Operator's Manual for information on how to use the Bar Code Reader.

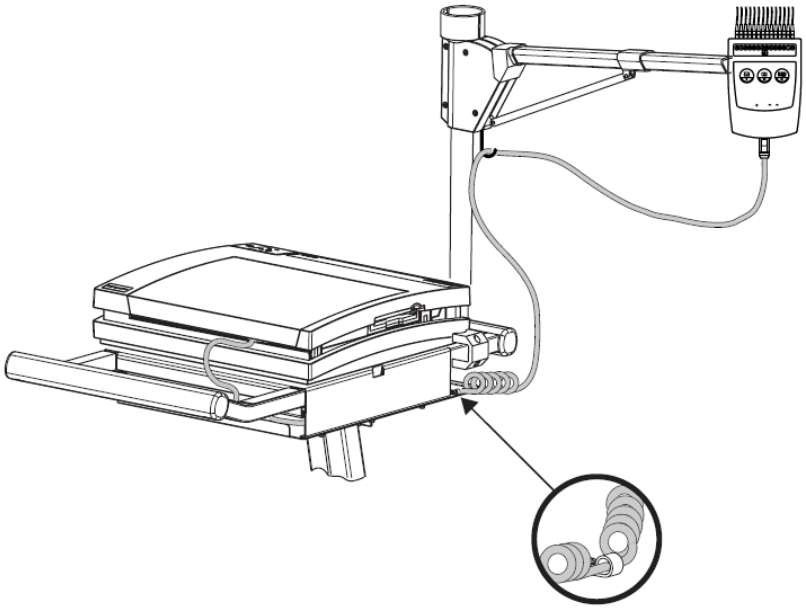
Type-S Trolley Assembly

1. To mount the MAC 5500 to the Type-S trolley, follow the steps in the illustration below.



75A

2. Route patient cable through trolley and fasten with cable clamp as shown below.



76A

MAC 5500 ST Requirements and Configuration

Following is a list of interface requirements and setup configurations required for the devices listed when used with the MAC 5500 ST option.

Compatible Blood Pressure Units

Colin - Model ST-780

Connection Requirements - Use cable PN 2008112-001 to connect from the MAC5500 port **1** to the Colin serial port. Use cable PN 2008111-001 to connect from the MAC 5500 **ANA/TTL** port to the Colin QRS trigger input.

Device Configuration Requirements - None

MAC 5500 Configuration Requirements – At the *Main Menu* complete the following in the order shown below:

- Select *System Setup*,
- Enter *System password*,
- *Exercise Test*,
- *Inputs/Outputs*,
- Change *Blood Pressure* to *Nipon-Colin*.

Sun Tech - Model Tango

Connection Requirements - Use cable PN 2008113-001 to connect from the MAC 5500 port **1** to the Sun Tech serial port. Use cable PN 2008111-001 to connect from the MAC5500 **ANA/TTL** port to the Sun Tech QRS trigger input.

Device Configuration Requirements – At the Tango Main Menu complete the following in the order shown below:

- Select *Utilities*,
- Select *Device*,
- Scroll to *ECG Trigger* and press enter,
- Scroll to *DIGITAL*↑ and press enter,
- Scroll to *EXIT* and press **Enter**,
- Scroll to *Test Parameters* and press **Enter**,
- With *Technique* highlighted, press **Enter**,
- Scroll to *DKA* and press **Enter**,
- Scroll to *EXIT* and press **Enter**,
- Scroll to *EXIT* and press **Enter** to return to the display screen.

MAC 5500 Configuration Requirements – At the *Main Menu* complete the following in the order shown below:

- Select *System Setup*,
- Enter *System password*,
- *Exercise Test*,
- *Inputs/Outputs*,
- Change *Blood Pressure* to *Suntech*.

Ergoline - Model Ergoline 900

Connection Requirements – Use cable PN 2008110-001 to connect from the MAC 5500 port **1** to the Ergoline serial port. Use cable PN 2008115-001 to connect from the MAC5500 **ANA/TTL** port to the Ergoline QRS trigger input.

Device Configuration Requirements – See Ergoline 900 Operator's Manual.

MAC 5500 Configuration Requirements – At the *Main Menu* complete the following in the order shown below:

- Select *System Setup*,
- Enter *System password*,
- *Exercise Test*,
- *Inputs/Outputs*,
- Change *Blood Pressure* to Ergoline Ergometer.

Compatible GE Medical Systems *Information Technologies* Treadmills

Model T2000

Connection Requirements – Use cable PN 2007918-001 (T2000) to connect from the MAC 5500 port **1** to the treadmill serial port.

Device Configuration Requirements – None.

MAC 5500 Configuration Requirements – Use the *Edit Protocol* application to set the protocol Test Type to *Treadmill in MPH* or *Treadmill in Km/H* for protocols that will be used with this treadmill.

Analog Treadmills

Connection Requirements – There are no cables available from GE Medical Systems *Information Technologies* to interface to analog treadmills. The customer is responsible for making the appropriate cable. Speed and grade signals for controlling analog treadmills are available on pins 2 (Slow Analog Output) and 8 (Fast Analog Output) of the **ANA/TTL** port. Pins 1, 4 and 5 are tied to ground.

Device Configuration Requirements – None.

MAC5500 Configuration Requirements – Use the Edit Protocol application to set the protocol Test Type to *Analog Treadmill in MPH* or *Analog Treadmill in Km/H* for protocols that will be used with this treadmill.

Configure pin 2 on the **ANA/TTL** port by selecting the following:

- *System Setup*,
- *Exercise Test*,
- *Inputs/Outputs*, and
- set *Slow Analog Output* to *Workload*.

Configure pin 8 on the **ANA/TTL** port by selecting the following:

- *System Setup*,
- *Exercise Test*,
- *Inputs/Outputs*, and
- Set *Fast Analog Output* to *Workload*.

Bicycle Ergometers

Ergoline 800/900, Lode Ergometer

Connection Requirements – Use cable PN 2008109-001 (Ergoline 800), PN 2008114-001 (Ergoline 900), or PN 2007981-001 (Lode Ergometer), to connect from the MAC 5500 **ANA/TTL** port to the ergometer analog control port.

NOTE

For any other ergometer, the customer is responsible for making the appropriate cable.

Device Configuration Requirements – Refer to ergometer Operator's Manual.

MAC 5500 Configuration Requirements – Use the *Edit Protocol* application to set the protocol Test Type to *Ergometer in Watts* or *Ergometer in KPM* for protocols that will be used with this ergometer.

Configure pin 2 on the **ANA/TTL** port by selecting the following:

- *System Setup*,
- *Exercise Test*,
- *Inputs/Outputs*, and
- *Slow* Analog Output to *Workload*, or
- Configure pin 8 by selecting:
  System Setup → *Exercise Test* → *Inputs/Outputs* → *Fast Analog Output to Workload*

For your notes

4 Troubleshooting

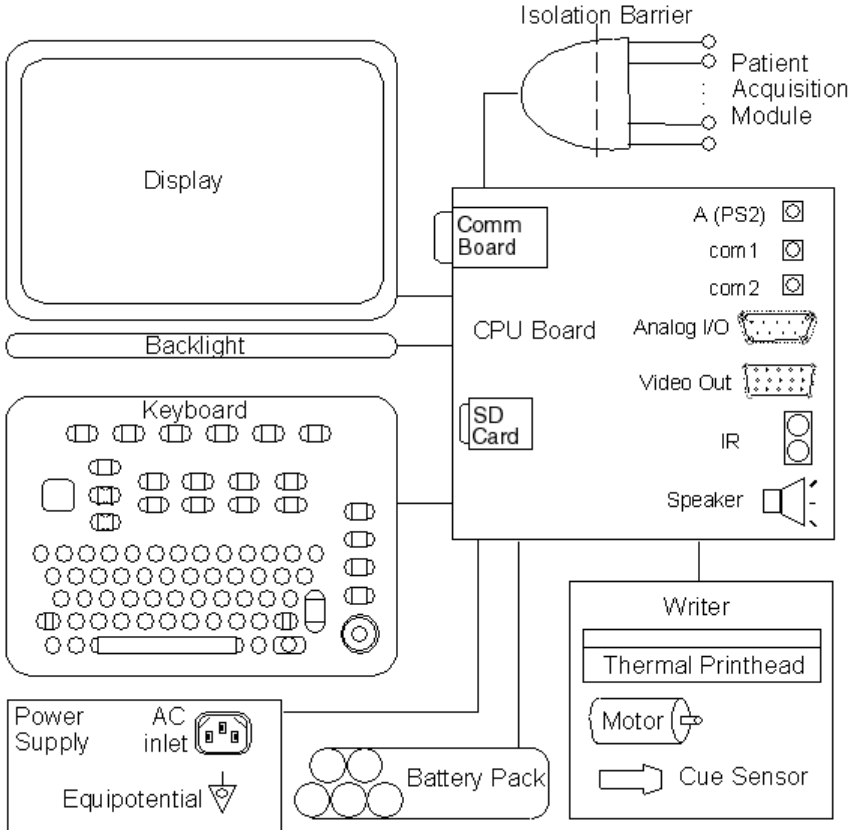
For your notes

Assembly Descriptions

Introduction

The troubleshooting information in this chapter helps you narrow service problems to one of the replaceable assemblies. These assemblies, illustrated in the block diagram, are discussed in more detail in the individual assembly chapters along with replacement procedures.

Assembly Block Diagram



General Fault Isolation

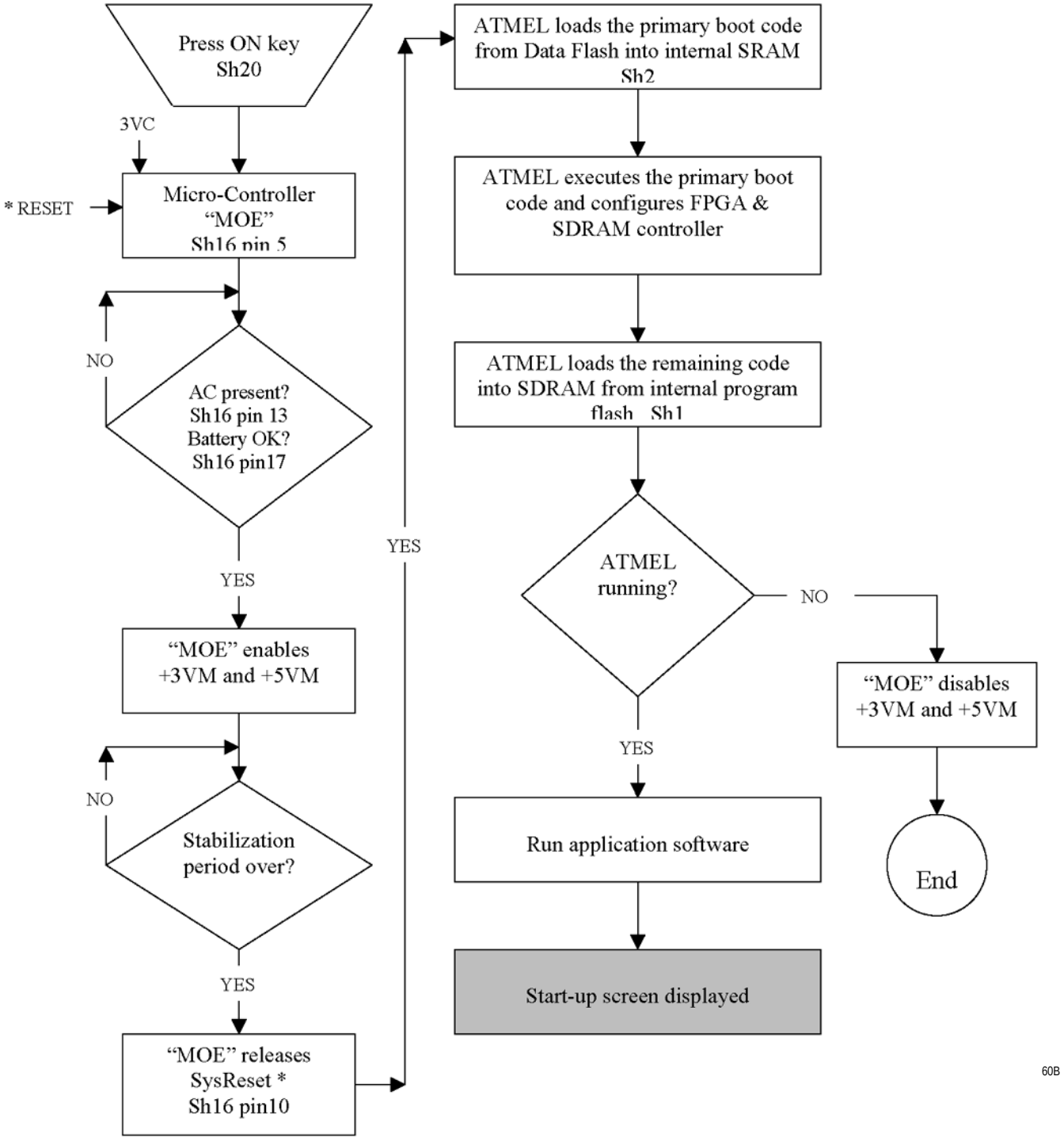
Power-up Self-test

See the MAC 5500 Operator's Manual, Chapter 2, "Equipment Overview: Getting Started" to verify operation.

On power-up, the system automatically runs an internal self-test. If all circuits test good, the start up screen displays. If the equipment is not working properly, ask yourself the following questions.

- Is the unit turned on?
- Have there been any changes in the use, location, or environment of the equipment that could cause the failure?
- Has the equipment hardware or software been modified since last use?
- Is operator error the cause of the problem? Try to repeat the scenario exactly and compare that to the proper operation of the equipment described in the manual.
- Is the battery installed?
- When connected to the AC wall outlet, does the green AC power light glow?
- Is the writer door closed?

Power-up Flow Chart



Poor Quality ECGs

Poor quality ECGs can be caused by factors in the environment, inadequate patient preparation, hardware failures related to the acquisition module, leadwires, cables, or problems in the unit.

Use a simulator to obtain an ECG report. If the report is good, the problem is external to the unit.

Visual Inspection

A thorough visual inspection of the equipment can save time. Small things—disconnected cables, foreign debris on circuit boards, missing hardware, loose components—can frequently cause symptoms and equipment failures that may appear to be unrelated and difficult to track.

NOTE

Take the time to make all the recommended visual checks before starting any detailed troubleshooting procedures.

Table 1. Visual Inspection List

Area	Look for the following problems
I/O Connectors and Cables	Fraying or other damage Bent prongs or pins Cracked housing Loose screws in plugs
Fuses	Type and rating. Replace as necessary.
Interface Cables	Excessive tension or wear Loose connection Strain reliefs out of place
Circuit Boards	Moisture, dust, or debris (top and bottom) Loose or missing components Burn damage or smell of over-heated components Socketed components not firmly seated PCB not seated properly in edge connectors Solder problems: cracks, splashes on board, incomplete feedthrough, prior modifications or repairs
Ground Wires/Wiring	Loose wires or ground strap connections Faulty wiring Wires pinched or in vulnerable position
Mounting Hardware	Loose or missing screws or other hardware, especially fasteners used as connections to ground planes on PCBs
Power Source	Faulty wiring, especially AC outlet Circuit not dedicated to system (Power source problems can cause static discharge, resetting problems, and noise.)

Diagnostic Tests

Introduction

Verify that the MAC 5500 resting ECG analysis system operates properly by running the diagnostic tests. These tests check the operation of the display screen, speaker, keyboard, thermal writer, battery, and communication. Detailed information displays on screen.

Loading the System Diagnostics

1. Select *Main Menu* on the Resting screen.
2. Select *More*.
3. Select *System Setup*.
4. At the prompt type the word “system”, the password set at the factory, then press the **Enter** key. If the password was not changed, the *System Setup* menu appears. If the menu does not appear, use the master password. If the system’s unique password is inaccessible, create one following the instructions in “Substitute Master Password” later in this section.
5. When the *System Setup* menu displays, hold down **Shift** and press **F5** (**Shift** + **F5**).
6. Type **prod** at the service password prompt.
7. The *System Diagnostics* menu appears.

Substitute Master Password

If you do not have access to the system’s password, you can create a master password as follows.

1. At the prompt for the system password, enter meimac. A random 6-digit number displays on the screen. For example, 876743.
2. Write the number down and create a new 6-digit number by adding alternating digits from the random number as follows. Add:
   - first and third digits,
   - second and fourth digits,
   - third and fifth digits,
   - fourth and sixth digits,
   - fifth and first digits, and
   - sixth and second digits.

   Disregard the 10s column when adding the digits. The new number from the example above would be 440020.
3. Enter the new number, then press the **Enter** key. The *System Setup* menu displays. This process only works once, so you should reprogram the password permanently.
4. Go to the *Basic System* menu.

5. Select *Miscellaneous Setup*.
6. Select the *System password* line and type the new password in the space.
7. Press the **Enter** key.
8. Select *Save Setup* from the *System Setup* menu.
9. Select *To system*.

System Diagnostics Main Menu

Use the arrow pad control to highlight a menu item, then press the **Enter** key to select it. The tests and test menus contain on-line prompts and/or instructions.

- *Display Tests*
- *Speaker Test*
- *Keyboard Test*
- *Writer Tests*
- *Battery Tests*
- *Communication Tests*
- *Acq. Module Tests*
- *Analog I/O Tests*
- *Floppy Drive Tests*
- *Internal Memory Tests*
- *SD Card Tests*
- *Exit System Diagnostics* (reboots the system)

Display Tests

Run the screen *Display Tests* to verify that all the screen pixels are working and that the brightness and contrast samples appear to be within normal range. There are no screen display adjustments. The screen *Display Tests* are as follows.

Pixel Verification Test

Use the arrow pad control to move the bar across the screen and look for any missing pixels on the display.

Press the **F1** key to turn on all of the pixels simultaneously.

Press the **Enter** key to exit the test.

Grey Scale Test Patterns

The first test pattern (used in manufacturing to verify the screen intensity) shows two squares, one bright and one dim. Press any key to activate the next display.

The second test pattern shows the 32-color text palette (Various gray scale patterns appear if the system does not have the color option enabled.). Check for problems with the overall pattern. (If the system does not have the color option, various grey scale patterns display.)

Press any key to exit the test.

Speaker Test

Use the arrow pad to select *Loud* or *Soft*. Press the **Enter** key to produce a loud or soft tone. (The tone level difference is minimal.)

If tone is not audible, the main CPU board may need replacement. (Speaker is part of CPU board.)

Highlight *Return* and press the **Enter** key to return to the *System Diagnostics* menu.

Keyboard Test

Press each key and verify that the key is highlighted on the screen and also displayed at the top of the screen. (It is normal for a dim background image to remain on the screen when you select the next key.) The numeric value that displays at the top of the screen is the scan code representation of the pressed key.

NOTE

The display shows keys in the upper part of the screen that are only available with the MAC 5500 ST keyboard.

- Check both of the **Shift** keys by pressing each in combination with a letter to display a capital letter.
- Press the center of arrow pad control and verify that the word *IN* displays on screen. Press **arrows** to change the displayed arrow position. A beep sounds with each arrow press.
- Press the **Shift** key and the **F6** key to exit the test.

Writer Tests

Run the writer tests to check the motor speed control, paper speed, paper tracking, paper cueing, and print head quality. During the tests, make the following general checks.

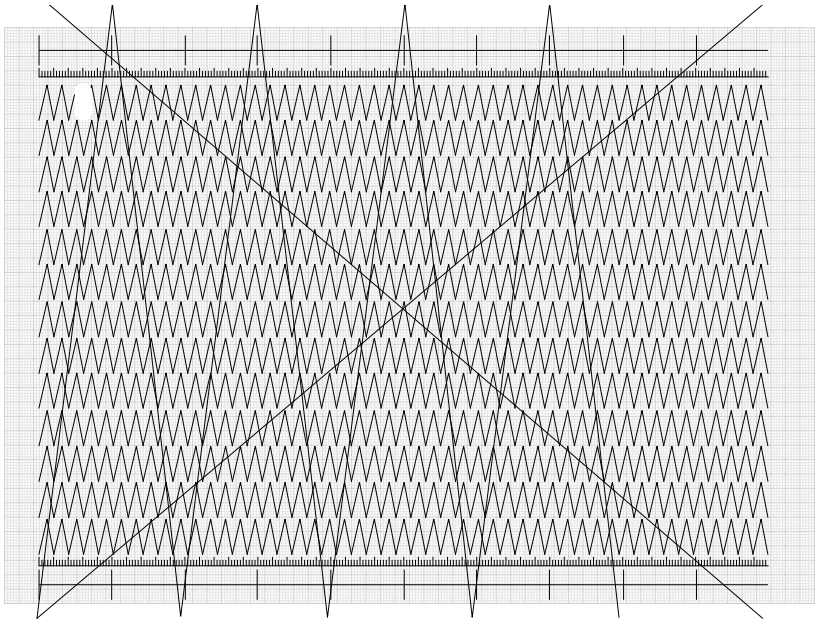
- The first character printed should not be distorted. This checks start-up speed.
- The writer should not skew or crush either edge of the paper.
- The large triangles and diagonal lines printed across the pages should be straight and uniform, without curves or wavering.
- The perforations should align with the tear bar on the door after cueing.
- Paper travel should be smooth.

C-Scan Tests 1, 2, & 3

These tests are combinations of test pattern I and the roller test. They are used by the writer vendor.

50 mm/s Test Pattern I, 25 mm/s Test Pattern I, and 5 mm/s Test Pattern I

These test patterns check the motor speed control and the paper speed. Verify that the length of the printout from start to finish is 250 mm ± 5 mm. Use the grids located on the top and bottom of the page for reference. Do this for each of the three tests.



61A

Roller Test

(Uneven darkness can appear if AC power is on during this test.)

- After cueing, printing should start at approximately 13–14 mm on the page.
- The pattern appears as diagonal light and dark wavy bands.

62A

- Isolated light spots indicate a flat spot on the roller and may indicate that the print carriage assembly needs to be replaced.
- A white line across the length of the page indicates a missing print head dot.

Test Pattern II

A combination of Test Pattern I and Roller tests. The first three pages consist of a series of triangular waveforms and various hashmarks. The fourth page is a partial roller test.

Test Pattern II Continuous

Test Pattern II runs continuously until **Stop** is pressed.

Continuously Run Out Paper

This test is used in manufacturing to test how well the unit self-corrects tracking problems.

Battery Tests

NOTE

The minimum discharge capacity is 2000 mAH. Consider replacing the battery if this number is less than 2000 mAH.

Battery Status

Displays, and constantly updates, the following information:

- Percent of charge remaining
- Battery voltage (With a reading of 80% or more for percent of charge remaining, the battery voltage should be between 15 and 24 volts. If battery voltage is below 15 volts, the battery may need to be replaced.)
- Battery current
  If battery current is less than -0.7 amps with AC power not applied, the main CPU may need to be replaced.
  (For example: Consider replacing the main CPU if the battery current is -0.8 amps with AC power not applied.)
- Battery temperature.
- Maximum and minimum battery temperature
- Ambient temperature (inside the unit).
  If the ambient temperature (inside the unit) is more than 10° greater than the current room temperature.
- Maximum and minimum ambient temperature
- Current battery charging status

Battery Discharge Test

This test charges the battery to full capacity, if necessary, then monitors a discharge cycle.

NOTE

To cancel the test at anytime, press the **ESC** key.

1. To perform the battery discharge test, plug the unit into AC (mains) power.
2. Select *Battery Discharge Test*. The battery discharge test window will appear and the unit will begin to charge the battery.
3. Once the battery is fully charged, the message *Turn the AC power to the unit OFF!* will appear.
4. Unplug the unit from AC (mains) power and select *OK*.
5. Re-select *Battery Discharge Test*. The battery will begin to discharge. When the battery has fully discharged, the unit will shut off.
6. Reconnect the unit to AC power and turn the unit on. Go to *Print Discharge Test Results*.

   Monitored information, written to the internal memory, includes:

   - Discharge capacity (in mAH)

- Battery temperature
- Battery charge status
- Percent of charge remaining

Battery Charge Test

This test completely discharges the battery, if necessary, then monitors a charge cycle.

NOTE

This test can take up to 6 hours to run. The “Battery Discharge Test” is a better indicator of the condition of the battery.

1. To perform the Battery Charge test, unplug the unit from AC (mains) power.
2. Select *Battery Charge Test*. The Battery charge test window will appear and the unit will begin to discharge the battery.
3. Once the unit has fully discharged the battery, plug the unit back into AC (mains) power. The battery will begin to charge.
4. When the battery charge test is complete, go to *Print the Charge Test Results*.

   Monitored information, written to internal memory, includes:

   - Charge rate (in mAH)
   - Battery temperature
   - Battery charge status
   - Percent of charge

Print Charge/Discharge Test Results

Prints the results of the last discharge or charge test to the writer.

Communication Tests

COM Port Loopback Test

The *Communications Port Loopback Test* sends various ASCII characters out the COM port’s transmit lines and expects the same character to return in it’s receive lines. Upon completion of the test, the word *Passed* or *Failed* appears, depending on the results.

For each of the options listed (COM1, COM2, COM3, and COM4) perform the following steps,

1. Select an option and press the **Enter** key.
2. Follow the instructions on screen and install loopback jumpers in the selected serial port.
3. Remove the loopback jumpers when the test is complete.

External Modem Test

Connect a modem to **COM 2** and select *External Modem Test*. The test returns the modem ID number, firmware rev, and current parameter settings. If communication with the modem is unsuccessful, the ID and firmware rev display *N/A*.

Internal Modem Test

Select *Internal Modem Test*. The *Internal Modem Interrogation* screen displays. The test returns the modem ID number, firmware rev, and current parameter settings. If communication with the modem is unsuccessful, the ID and firmware rev display *N/A*. Press any key to exit this test.

Ethernet Module Test

Select *Ethernet Module Test*. The *Ethernet Module Interrogation* screen displays. The test returns the device IP address and the subnet mask information. If the Ethernet module test is unsuccessful, the ID and firmware rev display *N/A*. Press any key to exit this test.

Acquisition Module Test

Follow the instructions on screen.

NOTE

A shorting bar is required to perform this test.

- Tests if the acquisition module is powered
- Tests if the acquisition module is communicating
- Displays the acquisition module lead wire noise
- Indicates when one of the three acquisition module buttons is pressed
- Displays software version of acquisition module

Analog I/O Tests

Analog Output Test

Follow the instructions on screen to monitor the analog outputs using an oscilloscope. The outputs monitored are:

- +12V
- DC Output 1
- DC Output 2
- ECG Output
- TTL Trigger Output

Four sets of outputs are possible. Select the output sets using the arrow pad.

For example, to test DCOut 1, connect oscilloscope to pin 2 and ground to pin 4 or 5 and select DCOut 2 0V and check oscilloscope for reading of 0 volts. repeat for other selections. If any of these readings do not match, CPU may need to be replaced.

Analog Input Test

Follow the instructions on screen to connect a DC power supply to the DC input pins of the **ANA/TTL** connector. The voltage of the DC input displays. If test fails, the main CPU board may need to be replaced.

DCOut Loopback Test

Follow the instructions on screen to connect the DC Outputs to the Analog Inputs. The test sends all possible values out the DC Outputs and confirms that the correct values are read from the Analog Inputs. A pass/fail result displays. If either test fails, the main CPU board may need to be replaced.

NOTE

Pin numbers refer to the **ANA/TTL** port.

ECGOut/QRSTrigger Loopback Test

Follow the instructions on screen to connect the ECG Output and QRS Trigger Output to the Analog Inputs. The test sends all possible values out the ECG Output and a square wave out the QRS Trigger Output. It confirms that the correct values are read from the Analog Inputs. A pass/fail result displays. If either test fails, the main CPU board may need to be replaced.

NOTE

Pin numbers refer to the **ANA/TTL** port.

Floppy Drive Tests

This test does not apply to the MAC 5500 system.

Follow the instructions on screen. A read/write test is performed on a formatted floppy disk and a pass/fail test result is displayed. Try another disk if this test fails. If this test continues to fail, contact GE Medical Systems-*Information Technologies* for service.

NOTE

The following test and the resultant values are for manufacturing use only and NOT intended for service of this device.

A head radial alignment and Azimuth alignment test is performed using an Accurite test disk (part number is displayed on screen). Alignment test values will be displayed.

Internal Memory Tests

This test checks the internal storage memory of the unit.

1. Select *Internal Memory Tests* from the *System Diagnostics Main Menu*.

   The number of bad blocks and the amount of free memory displays.

2. Press any key to continue.

   A prompt appears asking *Do you want to format Internal Memory?*

3. Press **F** to format and any other key to escape.

NOTE

Do not format the internal storage memory if it contains data which has not yet been transferred.

SD Card Tests

1. Insert SD card which is not write-protected.
2. Select *SD Card Tests*.
3. If test fails, replace SD card and repeat test.
4. If test still fails, CPU board may need to be replaced.

NOTE

Do not format the SD card if it contains data which has not yet been transferred.

Equipment Problems

ECG Data Noise

If the acquired ECG data displays unacceptable noise levels:

- Verify proper electrode placement.
- Verify proper electrode application. (Perspiration and dead skin must be removed from the electrode site.)
- Check for defective or out of date electrodes.
- Check for defective, broken, or disconnected leadwires.
- Check the patient's position. The patient should remain motionless during the acquisition of a resting ECG.

Missing ACI-TIPI Report

- ACI-TIPI is disabled.
  - Enable ACI-TIPI.
- The selected report is *without interpretation*.
  - Select *Interpretation* for the report.
- The ACI-TIPI required information is not entered.
  - Make sure the age range, gender, and chest pain complaints are entered.
- The patient was entered as pediatric.
  - Make sure you enter an age range less than 16.
- The original ECG was acquired in an electrocardiograph without the ACI-TIPI option.

No BP from External Device

- Check setup.
  - If Suntech, check protocol on Tango.
- Check cables (Serial and TTL).
- Check TTL trigger.

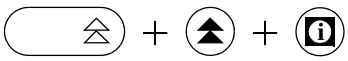
Treadmill/Ergometer Does Not Move

- Check protocol.
- Check cables.
- Check input / output settings.
- Check Emergency Stop switch.

System Errors

The following errors may occur while you are operating this system. You may be required to perform some action.

If you perform the recommended actions and the condition still remains, contact authorized service personnel. See “How to Reach Us” to find out how to contact GE Medical Systems *Information Technologies*.

Problem	Cause	Solution
appears on the screen.	No battery is installed in the system.	Install a battery and connect the system to an AC wall outlet to charge the battery.
flashes intermittently.	The battery charge is low.	Connect the system to an AC wall outlet to charge the battery.
appears on the screen.	The writer door is open.	Close the writer door.
The system does not power up when operating from battery power.	The battery is empty.	Connect the system to an AC wall outlet to charge the battery.
The system shuts down when operating from battery power.	Battery is empty, or the *Automatic Shutdown* feature is enabled.	Connect the system to an AC wall outlet to charge the battery, or power on the system.
“X” Lead disconnected message appears.	Electrode(s) disconnected.	Reconnect the electrode(s).
MODEM ERROR. The remote device is not responding. Would you like to retry?	Modem not connected. (If wireless option, client bridge not connected.)	Connect and retry.
	(Wireless option only) MAC 5500 is not within range of access point.	Relocate MAC 5500 to within range of access point and retry transmission.
Cannot use the system because *Device Password* does not work.	*Device Password* has been changed or has not been adequately communicated to the staff.	Override the *Device Password* prompt by pressing the following keys at the same time: 

63A, 64A, 65A

NOTE

For information about troubleshooting the MobileLink Standard Security option, see “MobileLink Installation & Troubleshooting Guide” (PN 2020299-021).

For information about troubleshooting the MobileLink Ultra High Security option, see “MobileLink UHS Installation & Troubleshooting Guide” (PN 2020300-051).

Frequently Asked Questions
Maintenance

NOTE
See Operator's Manual for complete *System Setup* information.

Save Setups

Q: How do I save changes I have made to the System Setups?

A: Check the following:

- Return to Menu by pressing the **esc** key or selecting *More* from the menu until you see *System Setup*.
- Select *System Setup*.
- Select *Save Setup*.
- Select *To System*.
- You can select *Main Menu* to exit *System Setup*.

Storing ECGs

Q: Why won't any of the ECGs I perform save to the SD card?

A: Check the following:

- Check that the SD card is fully inserted into the drive.
- Make sure you are using 64 MB SD cards.
- Verify that the SD card is not write-protected.
- Try a new SD card.
- If your system is not set up to automatically save records, you must manually save by pressing *Store*.

Format an SD Card

Q: How do I format an SD card in the MAC 5500?

A: Most secure digital cards do not require formatting. In the event an unformatted SD card is used with the system, the following message will display:

This SD Card cannot be read and requires formatting. Formatting will destroy all data on this SD Card. Are you sure you want to format?

Select *Yes* to format the SD card.

Cleaning

Q: Should I clean the MAC 5500?

A: Clean the exterior surfaces of all the equipment and peripheral devices monthly, or more frequently if needed.

- Use a clean, soft cloth and a mild dishwashing detergent diluted in water.
- Wring the excess water from the cloth. Do NOT drip water or any liquid on the writer assembly, and avoid contact with open vents, plugs, and connectors.

- Dry the surfaces with a clean cloth or paper towel.

Battery Capacity

Q: What is the capacity of the battery?

A: We recommend that the MAC 5500 be plugged into a wall outlet whenever it is not in use. However, the life of the battery is approximately 100 ECGs and one-page reports or six hours of continuous operation (without printing).

System Setup

Location Number

Q: When entering in the patient data, how do I get the Location field to automatically populate with the same number?

A: The *Location* number can be set in *System Setup* to save you from entering it for each test.

- Go to *System Setup*.
- Select *Basic System*.
- Select *Miscellaneous Setup*.
- Arrow down to *Location* and type in the number you want set as your default. Then press **Enter**.
- Press the **esc** key until you return to *System Setup*.
- Select *Save Setup*.
- Select *To System*.
- You can select *Main Menu* to exit *System Setup*.

Patient Questions

Q: How do I change what questions I see when I am entering the patient data?

A: The patient questions you see on the *Patient Data* window when starting a test were set up in *System Setup*.

- Go to *System Setup*.
- Select *Basic System*.
- Select *Patient Questions*.
- Select the patient questions you want to include when entering the patient data for a test.
- Press the **esc** key until you return to *System Setup*.
- Select *Save Setup*.
- Select *To System*.
- You can select *Main Menu* to exit *System Setup*.

Passwords

Q: Can you set up a password for the *Delete* function that is different than the *System Setup* password?

A: No. The password for the *System Setup* and the *Delete* function are the same.

Clinical

Report Format

Q: How do I change the way an ECG looks when it prints out?

A: Do the following steps.

- Go to *System Setup*.
- Select *ECG*.
- Select which type of ECG report you want to change:
  - *Resting ECG Reports*
  - *Pediatric ECG Reports*
  - *15 Lead Reports*
- Select unconfirmed reports from the menu.
- Find the report type you want the MAC 5500 to print.
- Place the number of copies you want in the appropriate column.
- If you want the MAC 5500 or 12SL interpretation included on the ECG, put the number of copies you want in the “with” column.
- If you do not want the MAC 5500 interpretation to print on the ECG, put the number of copies you want in the “without” column.
- Click view report type, to see the examples of the report formats.
- Press the **esc** key until you return to *System Setup*.
- Select *Save Setup*.
- Select *To System*.
- You can select *Main Menu* to exit *System Setup*.

Hi-Res and Phi-Res

Q: What is the difference between the Hi-Res and Phi-Res functions?

A: Hi-Res looks at the entire complex, whereas Phi-Res focuses on the P wave.

Editing

Q: Can you edit the interpretation at the MAC 5500, and then transmit the edited record to the MUSE system as an unconfirmed record?

A: If you edit demographic information only the record is still transmitted to the MUSE system as an unconfirmed record. However, if you edit the interpretation, the data will not be saved unless the record is confirmed at the MAC 5500. The record is transmitted to the MUSE system as a confirmed record as well.

Entering Patient Data

Q: Do I have to enter all the Information I see on the Patient Data screen?

A: In *System Setup* > *Basic System* > *Patient Questions* you can require that the patient identification number, or medical record number) be entered. It is not a requirement to enter any other data. However, we recommend that you enter the patient name and identification number, at the least. If you are transmitting to the MUSE system you will want to enter the *Location* number as well. If an emergency situation dictates that you must complete the test. without entering the patient data, make sure you edit the record to add the missing information before you transmit it to the MUSE system.

Transmission

Losing Fields When Transmitting

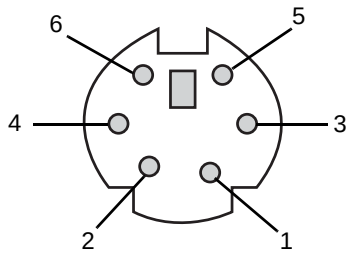
Q: Why do I lose the Referring MD and Technician names off of my reports when I transmit records to the MUSE system?

A: Your MAC 5500 may be transmitting to the SDLC modem on the MUSE system instead of the CSI modem. Check in System Setup to make sure you are transmitting to the MUSE system CSI phone number.

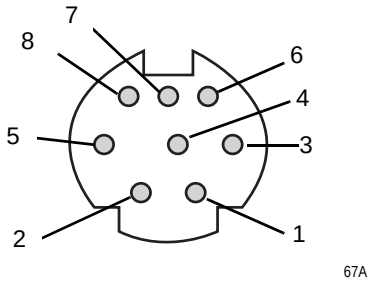
Input and Output Connectors

The following pages detail the input/output signals for those connectors. The pin-by-pin descriptions identify the signal names and pin outs for each connector on the unit.

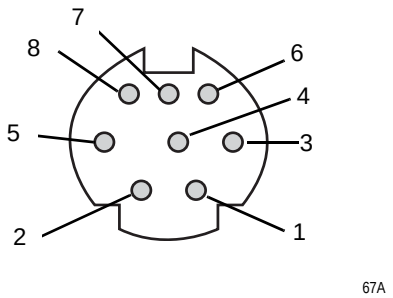
A Pins (J1)

Table 2. A Pins (J1)		
Pin	Name	
1	Data	
2	NC	
3	Ground	
4	+5V	
5	Clock	
6	NC	

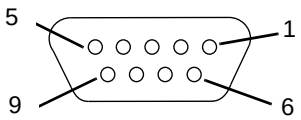
COM1 (COM3/4) Pins (J3)

Table 3. COM1 (COM3/4) Pins (J3)			
Pin	COM1 Signal	COM3/4 Signal	
1	RTS	COM3 TxD	
2	CTS	COM3 RxD	
3	TxD		
4	Ground		
5	RxD		
6	DTR	COM4 TxD	
7	+12V		
8	DSR	COM4 RxD	

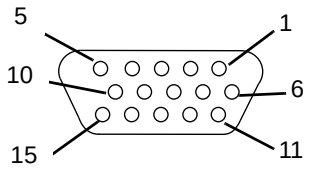
COM2 Pins (J5)

Table 4. COM2 Pins (J5)		
Pin	Name	
1	RTS	
2	CTS	
3	TxD	
4	Ground	
5	RxD	
6	DTR	
7	+12V	
8	DSR	

Analog Pins (J6)

Table 5. Acquisition Module Connector (J6)		
Pin	Name	
1	+12V	
2	DC Output 1	
3	TTL Trigger Output	
4	Ground	
5	Ground	
6	DC Output 2	
7	DC Input 1	
8	ECG Output	
9	DC Input 2	

EXT. VID. Pins (J7)

Table 6. External VGA Video (J7)		
Pin	Name	
1	Red Video	 68A
2	Green Video	
3	Blue Video	
4	Ground	
5	Ground	
6	Ground	
7	Ground	
8	Ground	
9	NC	
10	Ground	
11	Ground	
12	NC	
13	Horizontal Sync	
14	Vertical Sync	
15	NC	

CPU PCB Input/Output Signals

Battery Pack/Monitor, J2	
Pin No.	Signal
1	18V Battery Power
2	18V Battery Power
3	Battery Temperature Sense
4	3V Temperature Sense Power
5	Battery Ground
6	Battery Ground

LCD Backlight, J4	
Pin No.	Signal
1	12V Power
2	12V Power
3	12V Power
4	Ground
5	Ground
6	Brightness Select
7	Backlight Enable
8	NC
9	Ground
10	Ground

Keyboard, J8	
Pin No.	Signal
1	NC
2	NC
3	NC
4	NC
5	NC
6	Sense4
7	Sense2
8	Sense1
9	Sense0

Keyboard, J8 (Continued)	
10	Sense3
11	Sense5
12	Sense6
13	Sense7
14	Drive0
15	Drive1
16	Drive2
17	Drive3
18	Drive4
19	Ground
20	Power Key
21	Drive5
22	Drive6
23	Drive7
24	Drive8
25	Drive9
26	Drive10

LCD, J10	
Pin No.	Signal
1	Ground
2	Pixel Clock
3	Hsync
4	Vsync
5	Ground
6	R0 (LSB)
7	R1
8	R2
9	R3
10	R4
11	R5 (MSB)
12	Ground
13	G0 (LSB)
14	G1
15	G2
16	G3

LCD, J10 (Continued)	
17	G4
18	G5 (MSB)
19	Ground
20	B0 (LSB)
21	B1
22	B2
23	B3
24	B4
25	B5 (MSB)
26	Ground
27	Data Enable
28	3V Power
29	3V Power
30	NC
31	NC

Power Supply/Motor, J11	
Pin No.	Signal
1	Motor Encoder B
2	5V Power
3	Motor A
4	Motor Encoder A
5	Ground
6	Motor B
7	NC
8	28V Power
9	Ground
10	Battery Charge LED
11	28V Power
12	Ground
13	Door Open Detect
14	Ground

Thermal Printer, J12	
Pin No.	Signal
1	Thermal Printer Power
2	Thermal Printer Power
3	Thermal Printer Power
4	Thermal Printer Power
5	Thermal Printer Power
6	Thermal Printer Power
7	Thermal Printer Power
8	Ground
9	Ground
10	Ground
11	Ground
12	Ground
13	Ground
14	Ground
15	Cue Sense
16	NC
17	5V Main Power
18	Ground
19	Data Strobe
20	Data Strobe
21	Data Strobe
22	Data Strobe
23	Data Load
24	Data Clock
25	Print Head Temperature
26	Pixel Data

Floppy Disk Drive, J13 (for floppy drive — not installed	
Pin No.	Signal
1	5V Power
2	Index
3	5V Power
4	Drive Select 0
5	5V Power
6	Disk Change
7	NC
8	Media Sense 0
9	Media Sense 1
10	Motor Select 0
11	NC
12	Direction
13	NC
14	Step
15	Ground
16	Write Data
17	Ground
18	Write Gate
19	Ground
20	Track 0
21	Ground
22	Write Protect
23	Ground
24	Read Data
25	Ground
26	Head Select

Acquisition Module, J14	
Pin No.	Signal
1	Power
2	Ground
3	TX+ (RS485)
4	TX- (RS485)
5	RX+ (RS485)
6	RX- (RS485)
7	NC
8	NC
9	NC
10	NC

5 Maintenance

For your notes

Introduction

Recommended Maintenance

Regular maintenance, irrespective of usage, is essential to ensure that the equipment will always be functional when required.

WARNING
Failure on the part of all responsible individuals, hospitals or institutions, employing the use of this device, to implement the recommended maintenance schedule may cause equipment failure and possible health hazards. The manufacturer does not in any manner, assume the responsibility for performing the recommended maintenance schedule, unless an Equipment Maintenance Agreement exists. The sole responsibility rests with the individuals, hospitals, or institutions utilizing the device.

Required Tools and Supplies

In addition to a standard set of hand tools, you will need the items listed below.

Table 1. Tools and Supplies

Item	Part Number
#10 TORX driver	
Leakage current tester	MT-1216-02AAMI (for 220V) MT-1216-01AAMI (for 110V)
Multifunction micro-simulator	MARQ 1
Precision dust remover	
Lint-free soft cloth	TX609
PS2 style keyboard (Japan only)	

Inspection and Cleaning

Visual Inspection

Perform a visual inspection of all equipment and peripheral devices daily. Turn off the unit and remove power before making an inspection or cleaning the unit.

- Check the case and display screen for cracks or other damage.
- Regularly inspect all cords and cables for fraying or other damage.
- Verify that all cords and connectors are securely seated.
- Inspect keys and controls for proper operation.
  - Toggle keys should not stick in one position.
  - Knobs should rotate fully in both directions.

Exterior Cleaning

Clean the exterior surfaces monthly, or more frequently if needed.

1. Use a clean, soft cloth and a mild dish washing detergent diluted in water.
2. Wring the excess water from the cloth. Do not drip water or any liquid on the equipment, and avoid contact with open vents, plugs, or connectors.
3. Dry the surfaces with a clean cloth or paper towel.

Interior Cleaning

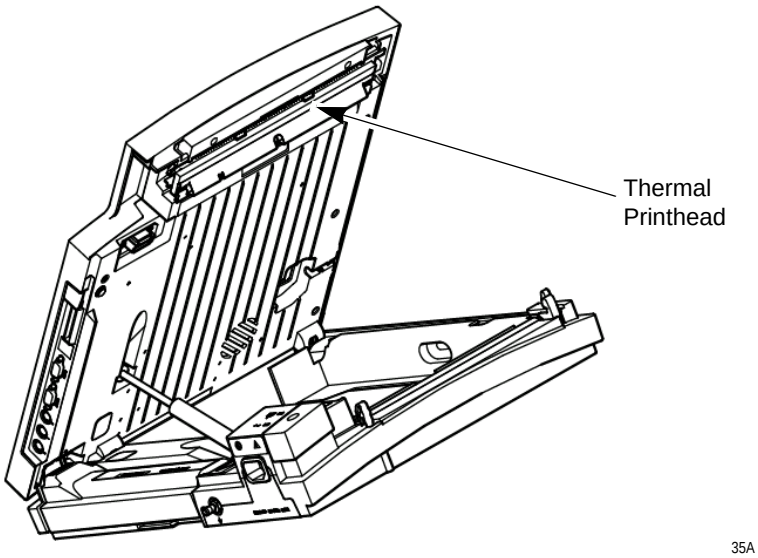
General

Check for dust buildup on the surfaces of the interior circuit boards, components, and power supply. Use commercially available compressed air to blow away the accumulated dust. Follow the manufacturers directions.

Thermal Printhead

Clean the thermal printhead every three months or more often with heavy use. A build-up of thermal paper coating on the printhead can cause light or uneven printing.

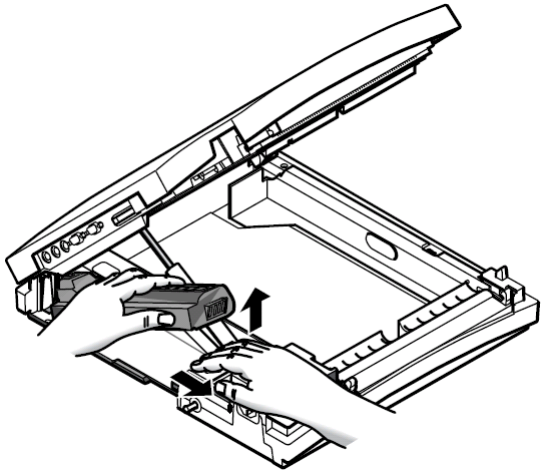
Use a solution containing alcohol on a nonwoven, nonabrasive cloth such as Techni-Cloth to wipe off the printhead. Do not use paper toweling, as it can scratch the printhead.


Thermal
Printhead
35A

Battery and Patient Cable Replacement

Battery Replacement

1. Press the internal access button to open the unit.
2. Slide the battery release button in the direction of the arrow and lift the battery out.

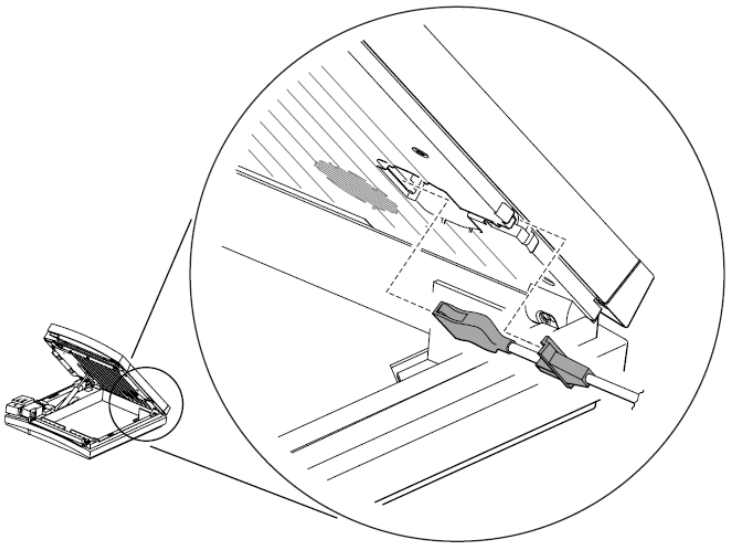


36A

3. Install a new battery and close the unit.

Patient Cable Replacement

1. Press the internal access button to open the unit.
2. Press the connector release tabs and pull the connector loose.
3. Pull the cable from the retaining tabs.



37A

4. Reassemble the cable by reversing the above steps.

Disassembly Guidelines

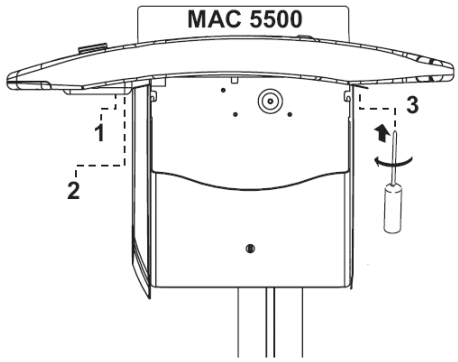
Preliminary Steps

Prior to disassembly, perform the following:

- If possible, process any ECGs remaining in storage.
- If possible, print out set-up for future reference.
- Disconnect the unit from the AC wall outlet and remove the power cord from the unit.
- Remove the battery.
- Remove the chart paper.
- Take strict precautions against electrostatic discharge damage.

Trolley Disassembly

1. Lock the wheels, remove the rear trolley panel then loosen the three captive screws located under the trolley.



21A

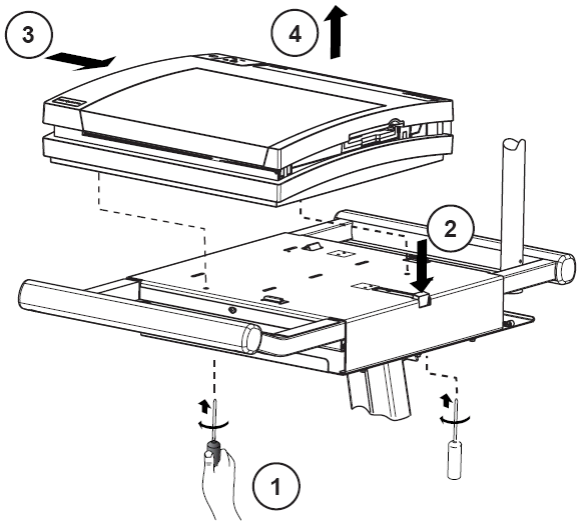
2. Pull the MAC 5500 up and up toward you.

20A

3. Lift the unit from the trolley.

Type-S Trolley Disassembly

To dismount the MAC 5500 from the Type-S trolley, follow the steps shown in the following illustration.

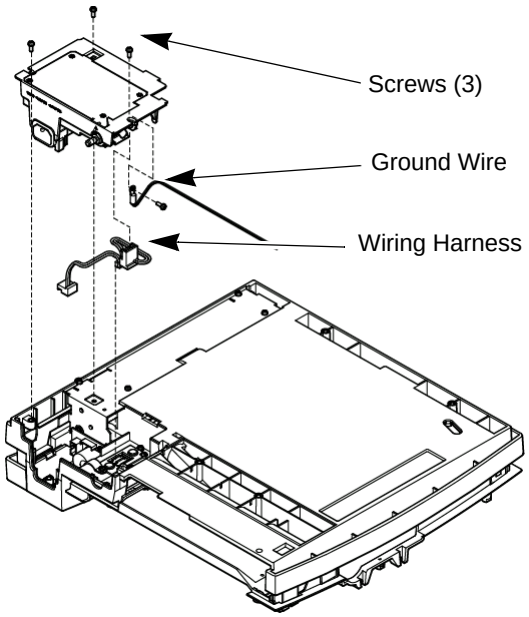


Power Supply

NOTE
A #10 TORX driver is required for disassembly and assembly of the power supply.

Removal

1. Turn the unit over so the bottom side is up.
2. Using a #10 TORX driver, remove the three screws holding the power supply in place.
3. Lift the power supply to expose the wiring harness and ground wire.
4. Remove P2 from J2 on the power supply assembly and the ground wire connection from the power supply chassis.



40A

Reassembly

Reassemble the power supply reversing the steps for removal. Before replacing the screws, ensure that the ground wire is routed through the notch in the plastic and not pinched.

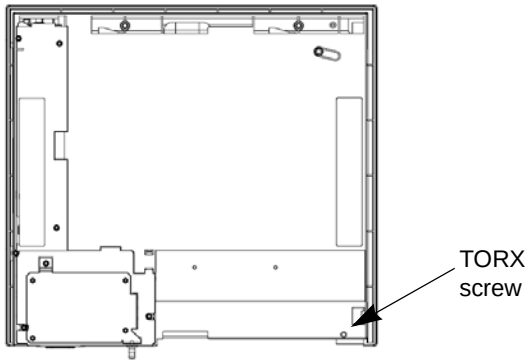
Top Cover

Removal

NOTE
It is not necessary to remove the Power Supply prior to removing the top cover.

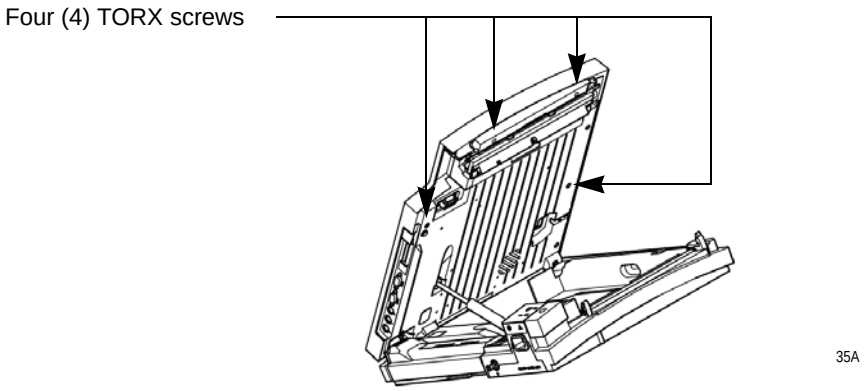
NOTE
A #10 TORX driver is required for disassembly and assembly of the top cover.

1. Remove the battery.
2. Turn the unit over so the bottom side is up and remove the TORX screw through the hole on the right rear corner of the unit. (This screw is only visible and accessible with the battery removed.)



41A

3. Turn the unit right side up and press the internal access button and raise the top of the unit.
4. Remove four (4) TORX screws.



5. Lower the top of the unit and lock in place.
6. Raise the display to the vertical position.
7. Gently lift the rear of the top cover free from the unit.

   NOTE

   The top cover holds the bezel that surrounds the rear panel connectors, so the bezel may fall free at this time.

8. At the front of the top cover, gently pull the thin strip of plastic free from under the keyboard. The entire top assembly is now loose.

   NOTE

   It may be helpful to rotate the top cover 45° to provide a larger opening to clear the display.

9. Carefully lift the top assembly up and clear of the raised display.

Reassembly

1. Raise the display to the vertical position.
2. Make sure the bezel surrounding the rear panel connectors is in place.
3. Lower the top cover down around the display and set in position.
4. Snap the rear of the top cover in place and then, gently pulling on the thin plastic strip at the front of the top cover, position it in place under the keyboard assembly.
5. Replace the screws removed in disassembly.

Display/Keyboard Assembly

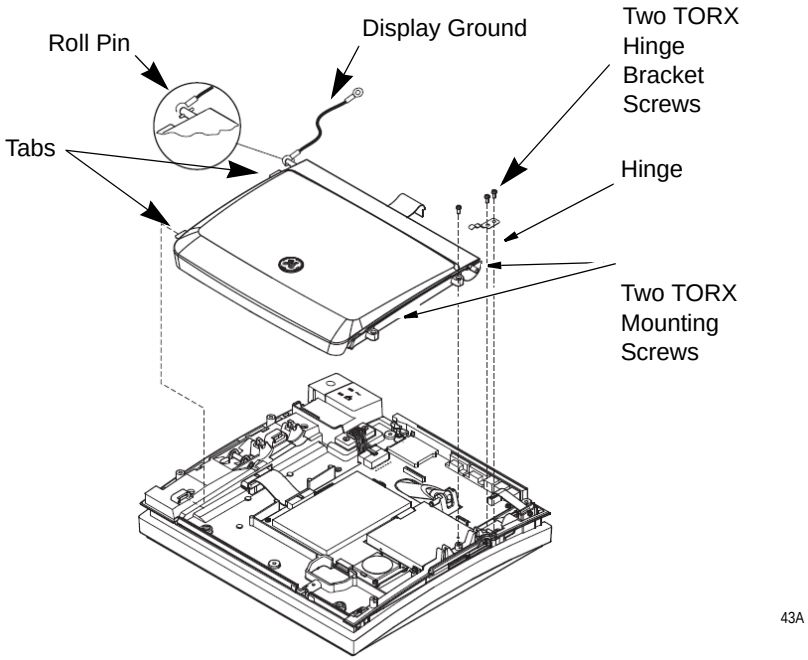
Removal

1. Remove the top cover following the procedures above.
2. Disconnect the three cables connecting the display/keyboard assembly to the main PCB.

   NOTE

   Two of these cables have locked connectors that must be lifted up to release the cables.

3. Working from the outside of the top, remove the two TORX mounting screws located on the right side of the assembly.
4. Remove the two TORX screws from the hinge bracket.
5. Remove the screw from the display ground at the left of the hinge rod.
6. Slide the display hinge (metal rod) to the left to release it from the mounting detent. A flat blade screw driver may be used to help slide the rod.

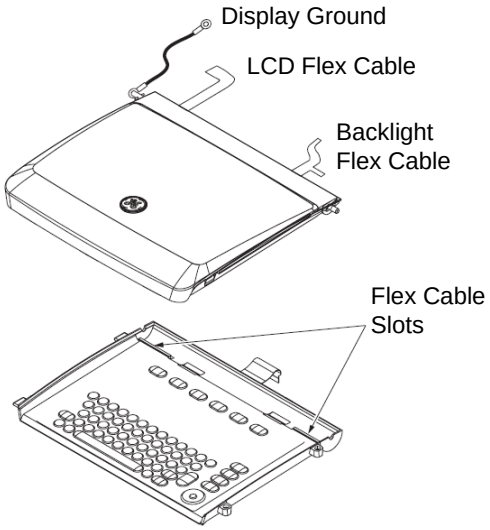


7. Slightly lift up on the right hand side of the display/keyboard assembly, and pull the assembly to the right to free the tabs from their mounting slots. Do not lift the right side of the display too high or the plastic tabs may be damaged.
8. When free from the main unit, the display/keyboard assembly can be separated in to two pieces allowing replacement of either the keyboard or display assembly.

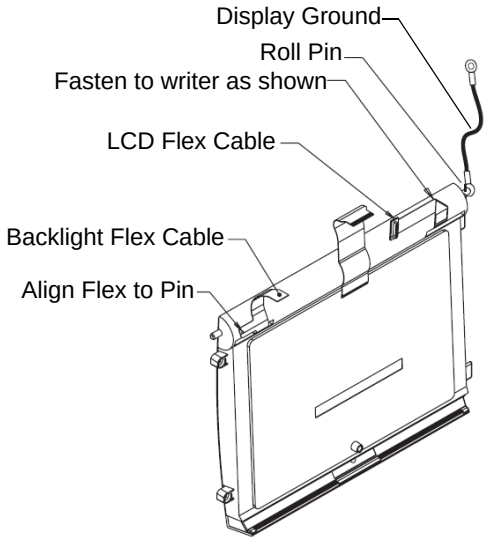
   NOTE

   Further disassembly of the LCD assembly is not recommended. Replace as complete assembly.

Display/Keyboard Reassembly



45A



44A

1. Insert both flex cables through flex cable slots and position them as shown.
2. Tilt the display/keyboard assembly to the left and with the roll pin of the hinge (metal rod) parallel to the left hinge base, insert the rod into the left hinge base and lower the display/keyboard assembly in place.
3. Slide tabs into their mounting slots and set the display/keyboard assembly in place.
4. Connect the three cables from the display/keyboard assembly to the main PCB. Be sure to lift the locks up prior to attempting to insert the cables into the connectors.
5. Slide the display hinge (metal rod) to the right until it locks into the right hinge base.
6. Replace the hinge bracket with the two TORX screws removed earlier.
7. Replace the screw and display ground at the left of the hinge rod.
8. Replace the two TORX mounting screws on the right side of assembly.

Reassembly

1. Raise the display to the vertical position.
2. Make sure the bezel surrounding the rear panel connectors is in place. Make sure the release mechanism for the Smartmedia card functions properly.
3. Lower the top cover down around the display and set in position.
4. Snap the rear of the top cover in place and then, gently pulling on the thin plastic strip at the front of the top cover, position it in place under the keyboard assembly.
5. Replace the screws removed in disassembly.

Main CPU Board

Removal of CPU Board

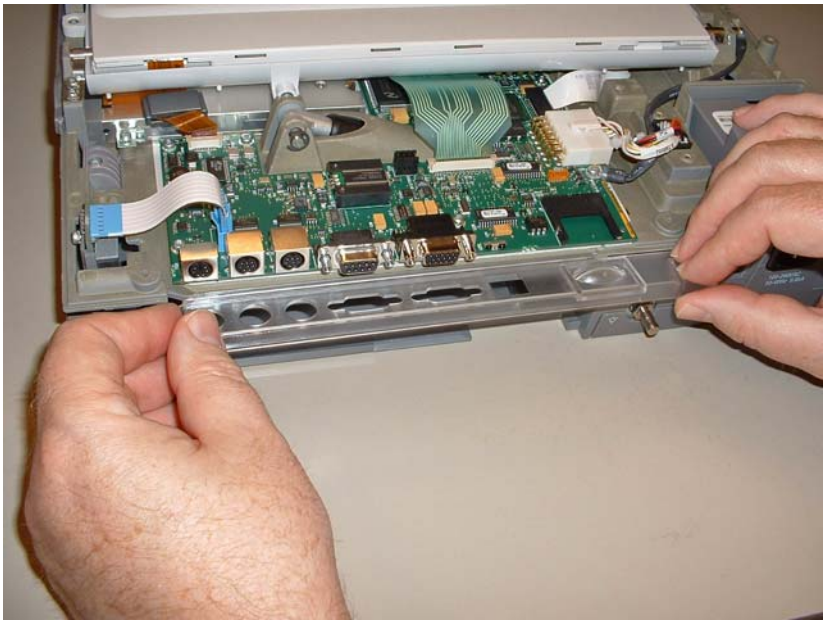
NOTE

Before you begin, save the current System Setups to an SD card and print System Setup report. This will be used to restore the system setups after replacement of the CPU board.

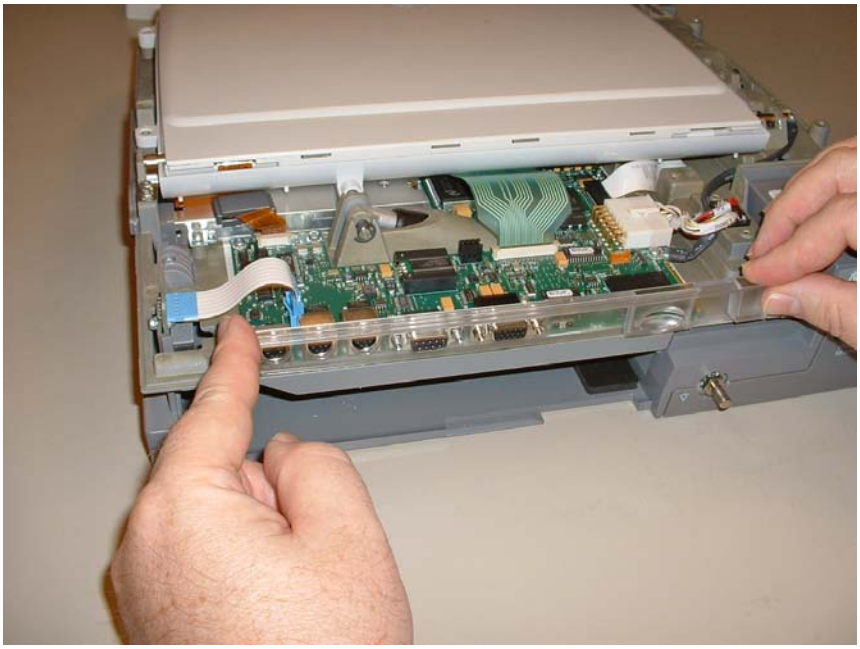
1. Remove the battery.
2. Remove the top cover assembly following the procedures in “Top Cover” on page 5-9.
3. Remove the display/keyboard assembly following the procedures in “Display/ Keyboard Assembly” on page 5-11.
4. Disconnect all remaining cable connections to the main PCB. These include cables to the following:
   - power supply
   - printhead
   - battery connect PCB
   - acquisition module cable
5. Remove the COMM board.
6. With a TORX driver, remove the mounting screws holding the main PCB in place. They are located around the outside edges of the main PCB. Set screws aside for mounting new board.
7. Remove the harness cable.
8. Lift the main PCB from the unit.

Reassembly of CPU Board

1. Insert the new CPU board in place and mount using the screws set aside during disassembly.
2. Reassemble the top cover and display/keyboard assemblies by reversing the steps for removal.
3. Insert rear bezel into slot on back of MAC 5500 assembly as shown below.



4. Rotate bezel to the upright position as shown below.



5. With the new bezel in place, replace the top cover by reversing the steps described previously.
6. Replace the battery and proceed with software, serial number, and system setups as described in the following sections.

Software

After replacing the CPU board, you need to install or update the software on the board as follows:

1. Connect the system to AC power.

   Keep the system connected to AC power during the software update and do not power off the system during the software update.

2. Press **Power** to turn on the system.
3. From the *Main Menu*, select *System Setup*.
4. Enter the system password. and press **Enter**.
5. Press **Shift** + **F3**.

   The following message is displayed.

   Please Insert SD Card

   Press 'Esc' to cancel

6. Insert the secure digital card with the application software.

   A message similar to the following displays.

   Current Version:

   New Software Version:

   Press 'Enter' to start installation

7. Press the **Enter** key.

   A series of messages that describe the update process displays.

   Copying code to Main Memory...

   Erasing Flash...Please Wait

   Programming Flash: 10 %

   One of three things happens at this point:

   - If the boot code is not being updated, the following message displays:

     Programming Over

     System is Shutting Down

   - If the boot code is being updated to a newer version, the following messages display:

Programming Primary Boot...

Programming Over

System is Shutting Down

- If the boot code is being downgraded to an earlier version, a message similar to the following message displays.

  Current Boot Version:

  New Boot Version:

  Press 'Enter' to start Installation

  Press **Enter**. The following messages display.

  Programming Primary Boot...

  Programming Over

  System is Shutting Down

8. Reboot the system and verify the software version.

Service Only Setups

1. From the *Main Menu*, select *System Setup*.
2. Press **Shift** + **F2** at the *System Setup* menu.
3. Enter the service password and press **Enter**.
4. The *Service Only Setup* window is displayed.

Service Only Setup

Serial number: _ _ _ _ _ _ _ _ _ _ _ _ _ _

Update Primary Boot: _ _ _

Print head resistance: _ _ _

Keyboard: _ _ _ _ _ _ _ _ _

Return

5. Enter the serial number of the system.

NOTE

This is the number which was used when the option codes for this system were generated. The number entered here must match the serial number on

the label of the system.

6. Select/verify that *No* is selected for *Update Primary Boot*.
7. Enter the *Print head resistance*. This number can be found on the print head label.
8. Select the appropriate language in the *Keyboard* menu.
9. Select *Return*.

Restore System Setups

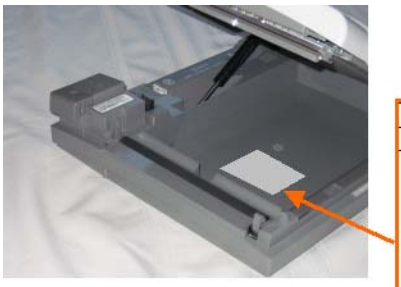
1. Power up the cart.
2. From the *Main Menu*, select *System Setup*.
3. Enter the *System Password* and press **Enter**.
4. Select *Restore Setup* from the *System Setup* menu.
5. Select *From SD Card* from the *Restore Setup* menu.

Restore Options

Using the option activation codes for the system, restore the options which had been installed on the board which was removed. These options are printed on a label located on the bottom of the paper tray.

NOTE

Use the activator codes shown on the label on your system. The activator codes shown in the figure below are examples only.



Serial # SCD04101589A	
Opcode	Activator Code
ST12	066062764546
ST15	541271375573
HRES	757166175301
PRES	775576210234
EDPR	570051503711
MODM	342671376664
FAXM	655447326375
DIAG	422733253021
RQRY	573705777537
TIPI	562707774425
GN12	645745743355
COLR	755316426645
MAST	624602777473
WIFI	717437704277
BCRD	354632773353
MGRD	226526500653
CTDG	736277035677
ELAN	776722553262

122A

1. Power on the cart.
2. Within the *System Setup* function, select *Basic System*.
3. Select *Option Activation* to activate options.
4. Type the 12-digit option activation code and press the **Enter** key.
5. Repeat the previous step for each option to be activated on the new system.

6. Highlight *Return* and press **Enter** to return to the *Basic System* menu.

Disable Options

It is possible to disable an option. In the rare instance you may need this functionality, follow these steps:

1. Within the system setup function, select *Basic System.*
2. Select *Option Activation*. The Option Activation screen displays.
3. In the entry field next to the option to be disabled, type "**x**" followed by the existing option code. The corresponding option will then be disabled.

   To re-enable the option, remove the "**x**" preceding the disabled option code.

Printhead Replacement

Removal

1. Remove the top cover following the procedure above.
2. Using a Phillips head screw driver, remove the two screws that hold the printhead to the printhead mounting plate.
3. Open the writer assembly, disconnect and remove the printhead.

Reassembly

1. Record the resistance value of the new printhead.
2. Connect the new printhead to the ribbon cable.
3. Hold the new printhead FIRMLY in place against the two metal tabs on the printhead mounting plate, then tighten the two screws.
4. Replace the top cover and power up the unit.
5. Go to the Setup menu and enter the new printhead resistance value.
6. Run a Writer Test test (See Chapter 5).

COMM Board Replacement

Use the following procedure to replace the communications board.

1. Remove the AC power cable and battery.
2. Using a Torx #10 screwdriver, remove the two screws from the panel surrounding the LAN and modem ports.

3. Grasp the side edges of the communications board and work it back and forth in the slot as you pull it out along its rails.

4. Insert the new communications board, sliding it onto the rails until it is seated in place.

5. Replace the panel surrounding the LAN and modem ports.
6. Replace the battery and AC power cable.

Setting up LAN Communications

After replacing the communications board, use the following procedure to set up the system's LAN communications.

NOTE:
Acquire the IP address, gateway, and subnet mask from the network administrator before beginning this process.

1. Power on the MAC system.
2. From the *Main Menu*, select *System Setup*.
3. If prompted, enter the system password.

   The default password is *system*.
4. From the *System Setup* menu, select *Basic System* > *Network Setup*.

   The *Network Setup* window opens.

5. Enter the *IP Address, Subnet Mask,* and *Gateway* provided by the network administrator
6. Enter the *Port Number* used by the MUSE system.
7. Select *Return* and press *Enter*.

   The Network Settings window closes.
8. On the Basic System menu, select Transmission and press Enter.

   The *Transmission* window opens.
9. Enter the following information.

Table 2. Transmission Information	
Field	Value
Use IR for serial line	No
Serial line baud rate	115.2K
Default location	Ethernet (MUSE)

10. Select *Return* and press *Enter*.

    The *Transmission* window closes.
11. On the *Basic System* menu, select *Return* and press *Enter*.

    The *Basic System* menu closes.
12. On the *System Setup* menu, select *Save Setup >To System*.

    This saves the settings to the communication board. This should take approximately 8 to 10 seconds. If it takes less than 8 seconds, the settings were not saved successfully. Repeat a second time.
13. Cycle power on the MAC 3500/MAC 5500 system.

    This ensures the network settings are reread from the communications board.
14. Wait at least 10 minutes and verify the MAC 3500/MAC 5500 can communicate with the MUSE system.

    Windows File Server 2000/2003 has an ARP cache that regenerates the MAC Address/Physical Address table every 10 minutes. When you replace the communications board, you change the MAC Address/Physical Address. By waiting at least 10 minutes, you allow the MUSE operating system to regenerate the MAC Address/Physical Address cache so the MAC 3500/MAC 5500 is able to communicate again with the MUSE system.
15. Perform all necessary functional checkouts.

Writer Roller/Carriage Assembly

Removal

1. Remove the power supply assembly following procedures above.
2. Inside the power supply compartment, disconnect the cable that connects to the writer assembly.
3. Open the unit to access the paper compartment. Move the paper size bracket to the A4 position to expose one of the writer assembly mounting screws.
4. Remove the screw and return the paper size bracket to the 8.5 x 11 position.
5. Close the unit and turn it over so the bottom side is up.
6. Remove the four screws located on the underside of the writer roller/carriage assembly and lift the writer from the bottom of the unit.

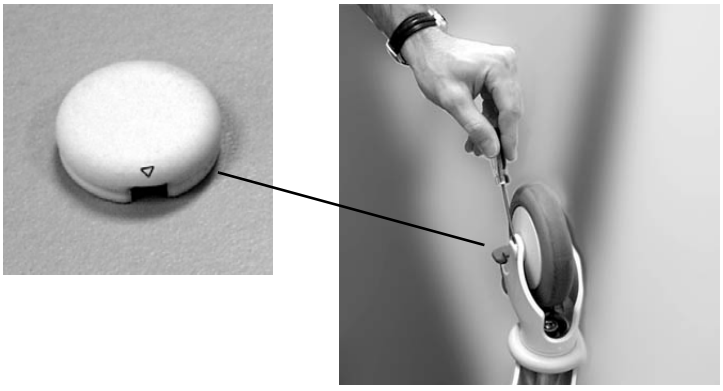
Reassembly

Reassemble the writer roller/carriage assembly by reversing the above procedures.

Trolley Casters

Removal

1. Remove the MAC 5500 and all loose items from the trolley and then place the trolley on its side.
2. Locate the slot under the arrow on the bearing dust cap and using a small blade screwdriver, pry the cap from the caster to be removed.



54A, 55A

3. Using an Allen wrench, remove the wheel shaft and wheel from the caster.

56A

4. Using an Allen wrench, remove the bolt holding the caster to the trolley.

57A

Reassembly

1. Install the replacement caster on the trolley.

   NOTE

   Ensure that the pins align with the holes on the fixed caster before fastening to the trolley.

57A, 58A

2. Install the wheel and attach with the wheel bearing shaft and nut.

56A

3. Using a small mallet, tap the bearing dust covers back in place.

59A

4. Set trolley upright and push to check alignment and free movement of casters.
5. Replace the MAC 5500 unit.

Functional Checkout Procedures

This checkout procedure applies to all MAC 5500 systems.

NOTE

The FRU checkout procedure for any listed FRU also applies to its internal PCBs and components. Perform the applicable product or product configuration dependant procedures when an asterisk * is listed.

Table 3. FRU Repairs

FRU Description	Tools	Visual Inspection	Checkout Procedure(s)
CAM 14	5	1,2,7	1,2,3
CAM 14 I/F Cable	5	1,2	1,2,3
Battery Pack	1,5	5	1,3,11
Shock Cylinder	1,2,4,5	9	1,3
Motherboard	1,2,3,4,5	3,5,9,10	1,2,3,4,13,20 *5 through 9
Roller Assy	1,2,4,5	9	1,2,3,15
Writer Assy	1,2,4,5	9	1,2,3,15
Display Assy	1,2,4,5	3,7,9	1,2,3,12
Keyboard Assy	1,2,4,5	3,9	1,2,3,14
Power Supply Assy	1,2,3,4,5	9,10	1,2,3
Plastics	1,2,3,4,5	7,9,10	1,3, *20 *Bottom Plastic Replacement Only
Trolley or Casters	2,5	6,9	10
AC Power Cord	3,5	4	1,3
Non-Listed FRUs	1,2,4,5	9,10	1,2,3,4,20 *5 through 9

Table 4. Option Repairs

FRU / Option	Tools	Visual Inspection	Checkout Procedure(s)
External Modem	1,2,5	9	1,3,5,17
Internal Modem (Comm PCB)	1,2,4,5	9	1,3,5,17
SD Card Storage	1,5,6	N/A	1,3,4,18

Table 4. Option Repairs (Continued)			
FRU / Option	Tools	Visual Inspection	Checkout Procedure(s)
Wireless Serial Server	1,2,5	9	1,3,5
LAN (Comm PCB)	1,2,5	9	1,3,5,19
Barcode Reader	1,2,5	9	1,3,8
Mag Card Reader	1,2,5	9	1,3,9
Treadmill or Ergometer I/F Cable	1,2,5	9	1,3,6
Blood Pressure Monitor	1,2,5	9	1,3

Table 5. Non-FRU Repairs			
Description	Tools	Visual Inspection	Checkout Procedure(s)
No Parts Replaced	1,5	1,2,3,4,5,6,7	1,3,4 *5 through 9
Software Update	1,5,6	N/A	1,2,3,4 *5 through 9
Hardware Upgrade	1,2,4,5	9,10	1,2,3,4,20 *5 through 9
Annual Electrical Safety Checkout	1,2,3,5	7,9,10	20, 1,2,3

Tools

1. ECG Simulator
2. Standard hand tools including a #10 and a #6 Torx Driver
3. Current Leakage Tester
4. Anti-static wrist strap
5. Applicable Service and/or Operator Manual as needed for reference
6. Floppy Diskette or SD Card

Visual Inspection

Inspect the following for excess wear and or any visual signs of damage.

1. Passed check for defective or broken patient cable/leadwires and out of date electrodes?
2. Discussed electrode placement, skin prep, and patient related requirements with ECG Tech?
3. Keyboard/LCD passed inspection?
4. AC Power cord passed inspection?
5. Battery (swollen or leaky) passed inspection?
6. Trolley and casters passed inspection?
7. External surfaces passed inspection?
8. FUSE type and rating passed inspection?
9. Fasteners replaced and secured?
10. All harnesses' and internal wiring has been secured?

Checkout Procedures

Perform the applicable checkout procedure.

Operational Checks

1. Power-up self-test passed?
2. Simulated recorded rhythm strip successful?
3. Simulated recorded ECG successful?
4. Simulated ECG stored on media successful?
5. Simulated ECG data transmitted successfully to MUSE?
6. Exercise device successfully communicates with MAC5500/5000?
7. Blood pressure monitor successfully communicates with MAC5500/5000?
8. Barcode reader successfully communicates with MAC5500/5000?
9. Magnetic card reader successfully communicates with MAC5500/5000?
10. Trolley casters lock successfully?

Diagnostic Tests

11. Battery Status Test meets Battery Current expectation?
12. Display diagnostic test successful?
13. Speaker test successful?
14. Keyboard test successful?
15. Writer diagnostic tests successful?
16. Read/Write Floppy Diagnostic Test successful? (Accurate test does not have to be performed)?
17. External/Internal Modem Test successful?
18. SD Card Test successful?
19. Ethernet Module Test successful?

Electrical Safety Checks

20. Current leakage and ground continuity test results meet requirements?

Perform electrical safety checks when indicated. All indicated electrical safety checks require a pass/fail indication for steps performed. Record the measurement values in your debrief.

Table 6. Electrical Safety Checks

Step		[1]Condition	[2]UUT - ON	Result		Leakage Current Limits
Earth Leakage Current						
1.	Forward Polarity	NC	_____ μA	Pass/Fail		300 μA
2.	Neutral open, Forward Polarity	SFC	_____ μA	Pass/Fail		1,000 μA
3.	Neutral open, Reverse Polarity	SFC	_____ μA	Pass/Fail		1,000 μA
4.	Reverse Polarity	NC	_____ μA	Pass/Fail		300 μA
Enclosure Leakage Current						
1.	Forward Polarity	NC	_____ μA	Pass/Fail		100 μA
2.	Neutral open, Forward Polarity	SFC	_____ μA	Pass/Fail		300 μA
3.	Ground open, Forward Polarity	SFC	_____ μA	Pass/Fail		300 μA
4.	Ground open, Reverse Polarity	SFC	_____ μA	Pass/Fail		300 μA
5.	Neutral open, Reverse Polarity	SFC	_____ μA	Pass/Fail		300 μA
6.	Reverse Polarity	NC	_____ μA	Pass/Fail		100 μA
Patient Leakage Current to Ground						
1.	Forward Polarity	NC	_____ μA	Pass/Fail		10 μA
2.	Neutral open, Forward Polarity	SFC	_____ μA	Pass/Fail		50 μA
3.	Ground open, Forward Polarity	SFC	_____ μA	Pass/Fail		50 μA
4.	Ground open, Reverse Polarity	SFC	_____ μA	Pass/Fail		50 μA
5.	Neutral open, Reverse Polarity	SFC	_____ μA	Pass/Fail		50 μA
6.	Reverse Polarity	NC	_____ μA	Pass/Fail		10 μA
Patient Leakage Current Mains on Applied Part[3]						
1.	Forward Polarity Neutral / Ground Closed	SFC	_____ μA	Pass/Fail		5000 μA
2.	Reverse Polarity Neutral / Ground Closed	SFC	_____ μA	Pass/Fail		5000 μA

Table 6. Electrical Safety Checks						
Step		[1]Condition	[2]UUT - ON	Result		Leakage Current Limits
Ground Continuity						Resistance
1.	AC mains power cord ground prong to exposed metal surface (ground lug)	N/A	_____ Ω	Pass/Fail		Less than 200mΩ

1. NC = Normal Condition
   SFC = Single Fault Condition
   N/A = Not Applicable
2. UUT = Unit Under Test
3. All SIPs/SOPs grounded.

For your notes

6 Parts List

For your notes

Ordering Parts

General Information

The FRU parts lists in this chapter supply enough detail for you to order parts for the assemblies considered field serviceable. To order parts, contact Service Parts at the address or telephone number on the, “How to Reach Us...,” page provided at the beginning of this manual.

Field Replaceable Units

The following items may not be assigned separate manufacturing part numbers because they are normally part of a larger assembly. Since they are considered field replaceable units (FRUs), they have specific service part numbers so they can be ordered and replaced by service technicians. Contact Tech Support for FRU information for assemblies used on previous configurations.

NOTE

Verify part numbers before ordering service parts (field replaceable units). See the tech memo series for this product for changes or additions to this list.

For Technical Support parts reference, see pn 2026609-001, MAC 5500 Assembly.

Field Replaceable Units	
Item	Part Number
Battery Assembly	900770-001
Power Supply Assembly	421117-001
Keyboard Assembly	421115-XXX
Display Assembly	2019106-001
Top Cover (See NOTE) Label Top Cover (See NOTE) NOTE: Top Cover & Label must be ordered together.	2017413-001 2008167-001
Printhead	422397-001
Writer Assembly	421108-006
Roller Assembly	422396-006
Writer Release Button	2005920-001
Leaf Spring	417565-001
Gas Cylinder	416015-001
Battery/LED Circuit Board	801222-001
MAC 5000 Country Modem PTO Option Class	MAC5000_MODEM
Country Specific (external modem)	2005264-0XX
MAC 5000 CAM14 PTO Option Class	MAC5000_CAM14
Kit CAM14 Resting ECG W/AHA Adapter	901142-001
Kit CAM14 Resting ECG W/IEC Adapter	901142-002
MAC5000 Keyboard PTO Option Class	MAC5000_KEYBRDS
Keyboard Assembly (Resting), English	421115-101
Keyboard Assembly (Stress), English	421115-201

Field Replaceable Units (Continued)	
Item	Part Number
Keyboard Assembly (Resting), German	421115-102
Keyboard Assembly (Stress), German	421115-202
Keyboard Assembly (Resting), French	421115-103
Keyboard Assembly (Stress), French	421115-203
Keyboard Assembly (Resting), Spanish	421115-104
Keyboard Assembly (Stress), Spanish	421115-204
Keyboard Assembly (Resting), Swedish	421115-105
Keyboard Assembly (Stress), Swedish	421115-205
Keyboard Assembly (Resting), Italian	421115-106
Keyboard Assembly (Stress), Italian	421115-206
Keyboard Assembly (Resting), Japanese	421115-107
Keyboard Assembly (Stress), Japanese	421115-207
Keyboard Assembly (Resting), Dutch	421115-108
Keyboard Assembly (Stress), Dutch	421115-208
Keyboard Assembly (Resting), Norwegian	421115-109
Keyboard Assembly (Stress), Norwegian	421115-209
Keyboard Assembly (Resting), Danish	421115-110
Keyboard Assembly (Stress), Danish	421115-210
Keyboard Assembly (Resting), Czech	421115-111
Keyboard Assembly (Stress), Czech	421115-211
Keyboard Assembly (Resting), Hungarian	421115-114
Keyboard Assembly (Stress), Hungarian	421115-214
Keyboard Assembly (Resting), Polish	421115-115
Keyboard Assembly (Stress), Polish	421115-215
Keyboard Assembly (Resting), Simplified Chinese	421115-113
Keyboard Assembly (Stress), Simplified Chinese	421115-213
Power Cord Generic PTO Option Class	POWERCORDS
Power Cord 125V 6FT Stress	80274-006
Power Cord 125V 6FT SE	80274-004
Power Cord CONT Euro 10A 250V 8FT	401855-001
Power Cord British 10A 250V 8FT	401855-002

Field Replaceable Units (Continued)	
Item	Part Number
Power Cord Italian 10A 250V 8FT	401855-003
Power Cord Israeli 10A 250V 8FT	401855-004
Wire Harness 10A 125V 6.5FT	401855-005
Wire Harness 10A 250V 6.5FT	401855-006
Power Cord Swiss 10A 250V 8FT	401855-007
Power Supply Cord, Indian 10A 250V 2.5M	401855-108
Danish 220VAC/50HZ,STRESS	401855-009
Power Cord Australian 10A 250V 8FT	401855-010
Power Cord 10A 8FT CONT Euro Stress	401855-101
Power Cord 10A 8FT British Stress	401855-102
Power Cord Italian 10A 8FT Stress	401855-103
Power Cord Israeli 10A 8FT Stress	401855-104
Power Cord Swiss 10A 8FT Stress	401855-107
Power Cord Indian 10A 8FT Stress	401855-108
Power Cord, Danish 10A 8FT Stress	401855-109
Power Cord AUST 10A 8FT Stress	401855-110
Power Cord 16A, Euro	401855-201
Power Cord 13A, British	401855-202
Power Cord 16A, Italian	401855-203
Power Cord 16A, Israeli	401855-204
Power Cord 15A AUST	401855-210
Cord Power Stress 125V 15A 12FT	405535-002
Cord Power RA 125V 13A 10FT	405535-006
Cord Power 18-3 SJT	5509-001
Power Cord RA 125V 13A 12FT	405535-001
Power Adapter 230VAC/DC ME	414582-222
Power Adapter 240VAC/DC AA	414582-224
Power Adapter 240VAC/DC, UK	414582-225
Power Cord European Adapter 1FT	415359-001
Power Adapter 100VAC/DC Japanese	414582-223
Barcode Scanner Kit, English	2018626-001

Field Replaceable Units (Continued)	
Item	Part Number
Barcode Scanner Kit, German	2018626-002
Barcode Scanner Kit, French	2018626-003
Barcode Scanner Kit, Spanish	2018626-004
Barcode Scanner Kit, Swedish	2018626-005
Barcode Scanner Kit, Italian	2018626-006
Barcode Scanner Kit, Norwegian	2018626-009
Barcode Scanner Kit, Danish	2018626-010
Barcode Scanner Kit, Czech	2018626-011
Barcode Scanner Kit, Hungarian	2018626-014
Barcode Scanner Kit, Polish	2018626-015
Kit 2D Barcode Imager MAC5000, English	2031240-001
Kit 2D Barcode Imager MAC5000, German	2031240-002
Kit 2D Barcode Imager MAC5000, French	2031240-003
Kit 2D Barcode Imager MAC5000, Spanish	2031240-004
Kit 2D Barcode Imager MAC5000, Swedish	2031240-005
Kit 2D Barcode Imager MAC5000, Italian	2031240-006
Kit 2D Barcode Imager MAC5000, Norwegian	2031240-009
Kit 2D Barcode Imager MAC5000, Danish	2031240-010
Kit 2D Barcode Imager MAC5000, Czech	2031240-011
Kit 2D Barcode Imager MAC5000, Hungarian	2031240-014
Kit 2D Barcode Imager MAC5000, Polish	2031240-015
Barcode Scanner Cable	2018629-001
Magnetic Card Reader Kit, English	2018627-001
Magnetic Card Reader Kit, German	2018627-002
Magnetic Card Reader Kit, French	2018627-003
Magnetic Card Reader Kit, Spanish	2018627-004
Magnetic Card Reader Kit, Swedish	2018627-005
Magnetic Card Reader Kit, Italian	2018627-006
Magnetic Card Reader Kit, Norwegian	2018627-009
Magnetic Card Reader Kit, Danish	2018627-010
Trolley Caster Fixed (Anti-Static)	2017784-002

Field Replaceable Units (Continued)	
Item	Part Number
Trolley Caster Swivel (Anti-Static)	2017785-002
Trolley Caster Kit (Anti-Static)	2024418-001
North American MobileLink Assembly (Ultra High Security)	2023922-001
North American MobileLink Assembly (Symbol)	2014403-002
European MobileLink Assembly (Symbol)	2014403-003
CPU Board NOTE: SD card with 9C software must be ordered with the CPU board. Earlier versions of the software will not work with the -007 board.	801212-007
CPU Board NOTE: This board is compatible with MAC5500s shipped with the -007 board. NOTE: Always reload the same or newer version of the software. Do not downgrade the software to a lower version.	801212-006
SD card with 9C software	2026831-003
PCB MAC3500 COMMS ROHS NOTE: SD card with 9C software must be ordered with the CPU board. Earlier versions of the software will not work with the -002 board.	2022332-002
PCB Comm Board (LAN, internal modem) NOTE: This board is not compatible with MAC5500s shipped with the -002 Comm board. NOTE: Always reload the same or newer version of the software. Do not downgrade the software to a lower version.	2022332-001
PCB Comm Board (LAN, internal modem) NOTE: This board is compatible with MAC5500s shipped with the -001 Comm board. NOTE: Always reload the same or newer version of the software. Do not downgrade the software to a lower version.	2022332-002
CAM 14 Acquisition Holder (for new trolley only)	2026528-001
SD card for external storage (128 MB)	2027268-001
SD card for external storage (256 MB)	2027268-002
SD card for external storage (512 MB)	2027268-003
#10 Torx Screws (M3 X 8MM TORX SEMS)	418545-001
Rear Bezel	2023119-001
Comm Board Guide	2025484-001
Assembly — Wireless Troy Serial Server (USA)	2026821-001[1]
Assembly — Wireless Troy Serial Server (Europe)	2026821-002[2]

Field Replaceable Units (Continued)	
Item	Part Number
FIPS Wireless Silex Serial Server (US government use only)	2047733-001
Assembly — Wireless Silex Serial Server (USA)	2034530-001
Assembly — Wireless Silex Serial Server (Europe)	2034530-002
Assembly — FIPS Wireless Silex Serial Server (US government use only)	2034530-003
Assembly — Wireless Silex Serial Server (USA)	2034529-001
Assembly — Wireless Silex Serial Server (Europe)	2034529-002
Power Supply — Wireless Troy / Silex Serial Server (for FIPS and non-FIPS)	2026825-001
Silex antenna (for FIPS and non-FIPS)	2038517-001
Power Supply — MAC 5000 Wireless (Symbol and Ultra High Security)	2013212-001

1. Replaced by and compatible with 2034530-001 (Silex Server USA)
2. Replaced by and compatible with 2034530-002 (Silex Server Europe)

Appendix A – Abbreviations

For your notes

Standard Abbreviations

A

A	ampere
A-ang	antianginal
A-arh	antiarrhythmic
A-coa	anticoagulants
A-hyp	antihypertensive
A1 - A4	auxiliary leadwires
AAMI	American Association of Medical Instrumentation
ABP	ambulatory blood pressure
ac, AC	alternating current
ACLS	Advanced Cardiac Life Support
A/D	analog-to-digital
Adj	adjustable
AG	automotive glass
Ah	ampere hours
AHA	American Heart Association
Al	aluminum
AllRam	all RAM
AllSec	all sector
AllTrk	all track
ALT	alternate
Alt-Off	alternate offset
am, AM	acquisition module, ante meridiem
AM-1	acquisition module-1
AM-1M	acquisition module-1 modified
AM-2	acquisition module-2
AM-3	acquisition module-3
AM-4	acquisition module-4
amp	ampere
Ampl	amplifier
AMU	ambulatory monitoring unit
ANA	analog
ANLG	analog
AnsrTone	answer tone
A/O	Analog Output
ASCII	American Standard Code for Information Interchange
ASSY	assembly
Attn	attention
AUG	August
AUST	Australian
AUSTRALN	Australian
Auto	automatic
AutoRhym	automatic rhythm
AUX	auxiliary
aVF	augmented left leg lead
avg	average
aVL	augmented left arm lead
aVR	augmented right arm lead
AWG	American Wire Gage

B

Bd	board, baud
BDGH	binding head
BetaB	beta blockers
BKSP	backspace
BLK	black
BLU	blue
Blvd	boulevard
BP	blood pressure
BPM	beats per minute
BRIT	Britain
BRN	brown
BSI	British Standards Institute
Btu	British thermal unit

C

CalcBlk	calcium blockers
CAPOC	Computer Assisted Practice of Cardiology
CASE	Computer Aided System for Exercise
Catoprl	Catopril
Cauc	Caucasian
Cer	ceramic
CFM	cubic feet/minute
CGR	computer graphic record
Ch, CH	channel
C/L	center line
CLK	clock signal
Clonid	Clonidine
cm	centimeter
cm^2	square centimeters
Cmd	command number
CMMR	common mode rejection ratio
CMOS	complementary metal-oxide semiconductor
c/o	in care of
COM1	communications port 1
COM2	communications port 2
ComLink	communications link
Comp	composition
Confrmd	confirmed
Cont, CONT	Continental, continued
Coumadn	Coumadin
CPR	cardiopulmonary resuscitation
CPU	central processing unit
CR	diode
CRC	cyclic redundancy check
CRD	cord
crt, CRT	cathode ray tube
CSA	Canadian Standards Association
CTRL	control

D

D/A	digital to analog
DA	damping relay
dac, DAC	digital-to-analog converter

DAN	Danish
Dat/Tim	date/time
dBm	decibel (referenced to 1 milliwatt into 600 ohms)
dc, DC	direct current
DD	double density, day
DDD	Digital Diagnostic Diskette
DEC	Digital Equipment Corporation, December
Del	delete
DEMO	demonstration
DES	designation
DevId	device identification
Diag	diagnostic
Digital	Digitalis
Digitox	Digitoxin
Digox	digoxin
Digoxin	Digoxin-Lanoxin
DIP	dual in-line package
Dirctry	directory
Diurt	diuretics
DOB	date of birth
DOS	disk operating system
DP	diametral pitch
DPST	double-pole, single-throw
DRAM	dynamic RAM
DR/DT	digital recording/digital transmission
DSKTP	desktop
Dysopyr	Dysopyramide

E

E	enable, vector electrode site, vector lead
ecg, Ecg, ECG	electrocardiogram
ECO	Engineering Change Order
EDIC	Electrocardiograph Digital Information Center
EEPROM	electrically erasable programmable ROM
e.g.	for example
EGA	enhanced graphics adapter
EMF	electromotive force
EMI	electromagnetic interference
ENG	English
EOF	end of file
EPIC	Electronic Patient Information Chart
EPLD	electrically programmable logic device
EPROM	eraseable, programmable, read-only memory
ESD	electrostatic discharge
etc, etc.	et cetera
EURO	Europe, European
EXP	Expanded

F

F	fuse, Farad, female
F1-F5	function keys 1 through 5
Fax	facsimile
FCC	Federal Communications Commission
FE	front end
FILH	fillister head

FLH	flat head
FLRAM	flash RAM
FR	French
FrntEnd	front end
FSK	frequency shift keying
ft	foot, feet
Furosem	Furosemide

G

g	gram, acceleration due to gravity
GB	Great Britain
GERM	German, Germany
GND	ground, digital ground (dc common)
GRN	green
GRY	gray

H

H	high, vector electrode site, vector lead
HDLC	high-level data link control
Hex, HEX	hexagon, hexadecimal
HH	hour
HiRes	high-resolution
Hr	hour
Hydral	Hydralazine
Hz	Hertz (cycles per second)

I

I	on, input, vector electrode site
I, II, III	limb leads
IC	integrated circuit
ID	identification
i.e.	that is
IEC	International Electrotechnical Commission
in	inch
IN	input
inc, inc., INC	incorporated
Info	information
Ins	insert
I/O	input/output
I/P	input
ISA	industry standard architecture
Isosorb	Isosorbide
IT	Italian, Italy

J

JAN	January
JIS	Japan Industrial Standards

K

k, K	kilo, 1000, 1024
Kb, KB	kilobyte
kg, Kg	kilogram
kHz, KHz	kilohertz
kV, KV	kilovolt

Kyb	keyboard

L

L	line
L1	level one
L2	level two
LA	left arm
lb	pound
LCD	liquid crystal display
Lcl Line	local line
Ld Grps	lead groups
LED	light-emitting diode
LH	left hand
Lidoca	Lidocaine
LL	left leg
Loc	location
LocPc	Local MAC PC
LogRetry	log retry
Ltd	limited

M

m	meter
M	megabyte, metric, vector electrode site, vector lead, male
mA	milliamperes
MAC	Microcomputer Augmented Cardiograph
mains voltage	voltage of a supply mains between 2 line conductors of a polyphase system or voltage between the line conductor and the neutral of a single-phase system
max	maximum
Measure	measurements
Med	medications
MEM	memory
MF	metal film
MHz	megahertz
min	minutes, minimum
Misc	miscellaneous
mm	millimeter
MM	minute
MMM	month
mm/mV	millimeter per millivolt
mm/s	millimeter per second
Modem	modulator/demodulator
MOS	metal oxide semiconductor
MPE	metallized polycarbonate expitaxial
ms	milliseconds
MS-DOS	Microsoft Disk Operating System
MTBF	mean time between failures
mtg	mounting
MTR	MOTOR
MUSE	Marquette Universal System for Electrocardiography
mux	multiplexer
mV	millivolt
mVR	minus (inverted) aVR

N

N	neutral
n/a	not available
NA	not applicable
NC	no connection
Nitrate	nitrates
NLQ	near letter quality
NMI	non-maskable interrupt
NMOS	N-channel metal-oxide semiconductor
No	number
NO	normally open
norm	normal
nS	nanoseconds
NSR	Normal Sinus Rhythm

O

O	off, original
OE	other errors
OEM	original equipment manufacturer
OH	off-hook relay
OneSec	one sector
ORG	orange
Orig	original
OUT	output
oz	ounce

P

P	P wave (section of the ECG waveform)
p-p	peak-to-peak
PA	P wave amplitude
Params	parameters
Passwds	passwords
PatData	patient data
PatInfo	patient information
PATN	patient
PC	printed circuit, personal computer
PCB	printed circuit board
pF	picofarad
Pgm	program
PgmId	program identification
Phenoth	Phenothiazide
Phenytn	Phenytoin
PID	patient identification digit
PLCC	plastic leadless chip carrier
PM	power module
pm, PM	post meridiem, preventive maintenance
PM-2	Power Module-2
PM-3	Power Module-3
pn, PN	part number
PNH	pan head
PPA	P wave amplitude
PR	ECG signal interval
Pro-Off	progressive offset
Procain	Procainamide
PROM	programmable read-only memory
Propran	Propranolol

PSK	phase shift keying
PSU	power supply unit
Psych	psychotropic
PUP	pull-up signal
PVC	polyvinyl chloride
PWM	pulse-width modulation
PWR	power
PWR CRD	power cord

Q

Q	transistor
QA	quality assurance, Q wave amplitude
QAD	Quality Assurance Deviation
QAM	quadrature amplitude modulation (phase and amplitude modulation)
QC	quality control
QD	Q wave duration
QRS	QRS complex (portion of ECG waveform), interval of ventricular depolarization
QT	QRS interval
QTC	QRS interval
QTY	quantity
Quinid	Quinidine

R

R	resistor, red, reset
RA	right angle, right arm or R wave amplitude
RAM	random access memory
RC	resistor capacitor
RD	R wave duration
Ref	reference, refresh
REN	Ringer Equivalence Number
Reserp	Reserpine
REV	revision
RevdBy	reviewed by
RevXmit	reverse transmission
rf	radio frequency
RFI	radio frequency interference
RGB	red, green, blue
RI	ring indicate
RL	right leg
RMR	Rhythm and Morphology Report
ROM	read only memory
RPA	R wave amplitude
RPD	R wave duration
rpt, Rpt	report
RTC	real time clock
RTI	relative to patient input
RTN	return
RVS	reverse
R/W	read/write

S

12SL	12 simultaneous leads

s, S	second, select, switch
SA	s wave amplitude
SB	slow-blow
SCL	safe current limits
SD	schematic diagram, S wave duration
SE	serial input/output errors
sec	second
sec.s	seconds
SEER	Solid-state Electronic ECG Recorder
SING	Singapore
SP	Spanish
SPA	S wave amplitude
SPDT	single-pole, double-throw
SRAM	static RAM
ST-T	ST-T wave (section of the ECG waveform)
standrd, Standrd	standard
STD	standard
STE	ST segment displacement at the end
STJ	ST segment displacement at the J point
STM	ST segment displacement at the mid-point between STJ and STE
stmts, Stmts	statements
supply mains	permanently installed power source
SVT	power cord type; 300 V
sw, SW	switch, software
SW	Swedish, Sweden

T

T Tone	touch tone
TA	T wave amplitude
Tant	tantalum
TDML	treadmill
TE	timeout errors
Tech	technical
Thiazid	Thiazide
TM	trademark
Tot	total
TP	test point
TPA	T’ wave amplitude
TRAM	Transport Remote Acquisition Monitor
Tricyli	Tricylic antidepressant
TTL	transistor-transistor logic, TTL levels
TVS	transient voltage suppressor

U

UE	undefined errors
uF	microfarad
UL	Underwriters’ Laboratory, Inc
Unconf	unconfirmed
UUT	unit-under-test

V

v, V	volt, volts
V1-V6	precordial leads
V123	V1, V2, V3

V3R	precordial lead
V456	V4, V5, V6
V4R	precordial lead
V ac	volts, alternating current
V dc	voltage, direct current
VA	volt-amperes
Var	variable
VDE	Verband Deutscher Elektrotechniker (German regulatory agency)
Vent.	ventricular
VF	ventricular fibrillation
VGA	video graphics array
VIA	versatile interface adapter
VIO	violet
Volt	voltage
VRAM	video RAM
vs	versus

W

w/	with
W	watt
Warfar	Warfarin
WHT	white
WI	Wisconsin

X

x	by (as in “8-1/2 x 11”)
XCV	transceiver
X,Y,Z	orthogonal leads

Y

Y	year, yellow
yr	year
yrs	years
YY	year

Symbols

↑	SHIFTed or alternate function
µ	micro
µF	microfarad
µs, µsec	microsecond
68K	68000
&	and
#	number
°C	degrees Celsius
°F	degrees Fahrenheit
Ω	Ohm, ohm
%	percent
®	registered
>	greater than
<	less than
±	plus or minus
*	An asterisk after a signal name indicates the signal is active at its relatively lower potential, or “active-low.” Signals without the

	asterisk suffix are active at their relatively higher potential, or "active-high."
12SL	12 simultaneous leads

Appendix B – Technical Specifications

For your notes

Technical Specifications

Display	
Item	Description
Type	264mm (10.4 in.) diagonal graphics backlit AM LCD
Resolution	640 x 480 pixels, with waveform enhancement
Displayed Data	Heart rate, patient name, ID, clock, waveforms, lead labels, speed, gain and filter settings, warning messages, prompts and help messages

Computerized Electrocardiograph	
Item	Description
Instrument Type	15 lead (14 channel) microprocessor-augmented, automatic electrocardiograph
Analysis Frequency	500 samples/s (sps)
ECG Storage	200 (maximum) on internal, non-volatile memory. Facility to archive ECG records on removable media (SD card).
Digital Sampling Rate	4000 samples/s/channel
Analysis	Pediatric and vectorcardiography Optional: 12SL analysis, HI-RES and PHI-RES late potential analysis
Pre-acquisition	Provides 10 s of instantaneous ECG acquisition
Dynamic Range	AC differential: ±5 mV DC offset: ±320 mV
Resolution	4.88 µV/LSB @ 250 sps, 1.22 µV/LSB @ 500 sps
Frequency Response	–3 dB @ 0.01 to 150 Hz
Common Mode Rejection	>140 dB (123 dB with AC filter disabled)
Input Impedance	>10 MΩ @ 10Hz, defibrillator protected
Patient Leakage Current	<10 µA
Pace Detection	750 µV @ 50 µs duration, Orthogonal LA, LL and V6
Special Acquisition Functions	Disconnected lead detection, electrode impedance, AC noise, baseline wander, and muscle tremor
Communication	MAC and MUSE system compatible RS-232 Optional: Modem, LAN, FAX, and wireless transmission, remote retrieval (remote query)

Writer	
Item	Description
Type	Thermal dot array
Speeds	5, 12.5, 25, 50 mm/s (same as display)
Number of Traces	3, 6, 12, or 15 user-selectable (same as display)
Sensitivity/Gain	2.5, 5, 10, 20, 10/5 (split calibration) mm/mV (same as display)
Speed Accuracy	± 2%
Amplitude Accuracy	± 5%
Resolution	Horizontal 1000 dpi @ 25 mm/s, 200 dpi vertical
Paper Type/Size	Thermal z-fold, perforated, 215.9 mm x 276.4 mm (8.5 in. x 11 in.) fanfold, 300 sheets per pack

Keyboard	
Item	Description
Type	Sealed elastomer with soft function keys, alphanumeric keys, writer controls and TrimPad cursor controls

Electrical	
Item	Description
Power Supply	AC or battery operation
AC Input Voltage Current Frequency	 100-240 VAC, +10, -15% 0.5 A @ 115 VAC, 0.3 A @ 240 VAC, typical 50/60 Hz, ±10%
Battery Type	User replaceable, 18V @ 3.5 AH ±10%, rechargeable NiMH pack
Battery Capacity	100 single-page reports (typical) or 6 hours continuous operation (without printing)
Battery Charge Time	Approximately 4.5 hrs. from total discharge with display off. NOTE: Cannot charge battery at or above 45° C (best if below 40° C)

Vectorcardiography	
Item	Description
Report Formats	Vector loops of component vectors (P, QRS, ST-T)
Sensitivity	20, 40, 80, 160 mm/mV
Time Resolution	2 ms

Hi-Res and PHi-Res Signal-Averaged Electrocardiography	
Item	Description
Frequency Response/Input	-3 dB @ 0.01 and 250 Hz
Frequency Response/Output Upper Limit Lower Limit	 250 Hz 0.01, 25, 40 or 80 Hz
Sensitivities Raw Data and Template Average Beat Filtered Signals and Vector Magnitude	 20 mm/mV 20 mm/mV and 50 mm/mV 1 mm/µV
Analysis Sampling Rate	1000 samples per second per channel
Digital Sampling Rate	4000 samples per second per channel
High/Low Pass Filters	Spectral filter using Fast Fourier Transform (FFT)
ADC Resolution	1.22 µV/LSB
Analysis Resolution	0.1525 µV/LSB

Physical [1]	
Item	Description
Height	9.4 cm (3.7 in) with display closed
Width	38.1 cm (15.0 in)
Depth	35.1 cm (13.8 in)
Weight	6.8 kg (15 lb) without paper

1. without trolley

Environmental	
Item	Description
Operating Conditions Temperature Relative Humidity Atmosphere Pressure	 10° C to 40° C (50° F to 104° F) [1] 20% to 95% RH noncondensing 700 to 1060 hPa

Environmental (Continued)	
Item	Description
Transport/Storage Conditions Temperature Relative Humidity Atmosphere Pressure	 -40° C to 70° C (-40° F to 158° F)* 15% to 95% RH noncondensing 500 to 1060 hPa
Disposal Batteries Device	 Disposing of battery by fire or burning will cause the battery to explode. The battery is recyclable. Follow local environmental guidelines concerning disposal and recycling. Batteries may be returned to GE Medical Systems *Information Technologies* service for recycling. Recyclable.

1. Paper discoloration may occur at higher temperatures.

Safety	
Item	Description
Certification	UL 60602-1 classified UL classified for CAN/CSA C22.2 No. 601.1 CB certified for IEC 60601-1 CE marking for Council Directive 93/42/EEC concerning Medical Devices Meets applicable AAMI EC-11 requirements
Type of Protection Against Electrical Shock	Class 1, internally powered
Degree of Protection Against Ingress of Liquids	Ordinary
Handling of Disposable Supplies and Other Consumables	Use only parts and accessories manufactured or recommended by GE Medical Systems *Information Technologies*. Follow manufacturer's instructions for use for disposable/ consumable products. Follow local environmental guidelines concerning the disposal of hazardous materials.
Patient Mode of Operation	Continuous
Patient Leakage Current	<10 µA
Degree of Protection Against Electrical Shock	Type BF defibrillation protection for the patient cable (acquisition module)
Maintenance Frequency	Daily visual inspection and routine cleaning (if needed) performed by user. Use a commercially available, industrial strength disinfectant cleaner on any part of the equipment (other than electrodes) which comes into direct contact with the patient. Every six months routine maintenance checks and test procedures performed by qualified technical personnel.
Repair Guidelines	Calibration instructions, equipment descriptions, and all other information which will assist qualified technical personnel in repairing those parts of the equipment designated as repairable is available in the field service manual for the equipment. We will make available upon request circuit diagrams and component parts lists for printed circuit boards deemed repairable by qualified technical personnel.

For your notes

Appendix C – Electromagnetic Compatibility

For your notes

Electromagnetic Compatibility (EMC)

Changes or modification to this system not expressly approved by GE Medical Systems could cause EMC issues with this or other equipment. This system is designed and tested to comply with applicable regulation regarding EMC and needs to be installed and put into service according to the EMC information stated as follows.

WARNING
Use of portable phones or other radio frequency (RF) emitting equipment near the system may cause unexpected or adverse operation.

WARNING
The equipment or system should not be used adjacent to, or stacked with, other equipment. If adjacent or stacked use is necessary, the equipment or system should be tested to verify normal operation in the configuration in which it is being used.

Guidance and Manufacturer's Declaration - Electromagnetic Emissions

The MAC 5500 is intended for use in the electromagnetic environment specified below. It is the responsibility of the customer or user to ensure that the MAC 5500 is used in such an environment.

Emissions Test	Compliance	Electromagnetic Environment - Guidance
RF emissions CISPR11	Group 1	The equipment uses RF energy only for its internal function. Therefore, its RF emissions are very low and are not likely to cause any interference in nearby electronic equipment.
RF emissions CISPR11	Class A	Class A Equipment is suitable for use in all establishments other than domestic and those directly connected to the public low-voltage power supply network that supplies buildings used for domestic purposes.
Harmonic Emissions EN 61000-3-2	Class A	
Voltage fluctuations/ Flicker emissions EN 61000-3-3	Complies	

Guidance and Manufacturer's Declaration - Electromagnetic Immunity

The MAC 5500 is intended for use in the electromagnetic environment specified below. It is the responsibility of the customer or user to ensure that the MAC 5500 is used in such an environment.

Immunity Test	EN 60601 Test Level	Compliance Level	Electromagnetic Environment - Guidance
Electrostatic discharge (ESD) EN 61000-4-2	± 6 kV contact ± 8 kV air	± 6 kV contact ± 8 kV air	Floors should be wood, concrete or ceramic tile. If floors are covered with synthetic material, the relative humidity should be at least 30%.
Electrical fast transient/burst EN 61000-4-4	± 2 kV for power supply lines ±1 kV for input/output lines	± 2 kV for power supply lines ±1 kV for input/output lines	Mains power should be that of a typical commercial or hospital environment.
Surge EN 61000-4-5	± 1 kV differential mode ± 2 kV common mode	± 1 kV differential mode ± 2 kV common mode	Mains power should be that of a typical commercial or hospital environment.
Voltage dips, short interruptions and voltage variations on power supply input lines EN 61000-4-11	<5% Ut (>95% dip in U_t) for 0.5 cycles 40% Ut (60% dip in U_t) for 5 cycles 70% Ut (30% dip in U_t) for 25 cycles <5% Ut (>95% dip in U_t) for 5 sec	<5% Ut (>95% dip in U_t) for 0.5 cycles 40% Ut (60% dip in U_t) for 5 cycles 70% Ut (30% dip in U_t) for 25 cycles <5% Ut (>95% dip in U_t) for 5 sec	Mains power should be that of a typical commercial or hospital environment. If the user of the MAC 5500 requires continued operation during power mains interruptions, it is recommended that the MAC 5500 be powered from an uninterruptible power supply or a battery.
Power frequency (50/60 Hz) magnetic field EN 61000-4-8	3 A/m	3 A/m	Power frequency magnetic fields should be at levels characteristics of a typical location in a typical commercial or hospital environment.

NOTE

Ut is the AC mains voltage prior to application of the test level.

Guidance and Manufacturer's Declaration - Electromagnetic Immunity

The MAC 5500 is intended for use in the electromagnetic environment specified below. It is the responsibility of the customer or user to assure that the MAC 5500 is used in such an environment.

Immunity Test	EN 60601 Test Level	Compliance Level	Electromagnetic Environment – Guidance
			Portable and mobile RF communications equipment should not be used closer to any part of the equipment, including cables, than the recommended separation distance calculated from the equation applicable to the frequency of the transmitter. Recommended separation distance
Conducted RF EN 61000-4-6	3 Vrms 150 KHz to 80 MHz	3 V rms	$d = 1.2\sqrt{P}$
Radiated RF EN 61000-4-3	3 V/m 80 MHz to 2.5 GHz	3 V/m	$d = 1.2\sqrt{P}$ 80 MHz to 800 MHz $d = 2.3\sqrt{P}$ 800 MHz to 2.5 GHz where **P** is the maximum output power rating of the transmitter in watts (W) according to the transmitter manufacturer, and **d** is the recommended separation distance in meters (m). Field strengths from fixed RF transmitters, as determined by an electromagnetic site survey[a], should be less than the compliance level in each frequency range[b]. Interference may occur in the vicinity of equipment marked with the following symbol:

NOTE 1: At 80 MHz and 800 MHz, the higher frequency range applies.
NOTE 2: These guidelines may not apply in all situations. Electromagnetic propagation is affected by reflection from structures, objects, and people.

[a] Field strengths from fixed transmitters, such as base stations for radio (cellular/cordless) telephones and land mobile radio, AM and FM radio broadcast, and TV broadcast cannot be predicted theoretically with accuracy. To assess the electromagnetic environment due to fixed RF transmitters, an electromagnetic site survey should be considered. If the measured field strength in the location in which the equipment is used exceeds the applicable RF compliance level above, the equipment should be observed to verify normal operation. If abnormal performance is observed, additional measures may be necessary, such as re-orienting or relocating the equipment.

[b] Over the frequency range 150 KHz to 80 MHz, field strengths should be less than 3 V/m.

Recommended Separation Distances

The table below provides the recommended separation distances (in meters) between portable and mobile RF communication equipment and the MAC 5500.

The MAC 5500 is intended for use in the electromagnetic environment on which radiated RF disturbances are controlled. The customer or the user of the MAC 5500 can help prevent electromagnetic interference by maintaining a minimum distance between portable and mobile RF communications equipment (transmitters) and the MAC 5500 as recommended below, according to the maximum output power of the communications equipment.

	Separation Distance in Meters (m) According to Frequency of Transmitter			
Rated Maximum Output Power of Transmitter in Watts	150 kHz to 80 MHz outside ISM bands $d = 1.2\sqrt{P}$	150 kHz to 80 MHz in ISM bands $d = 1.2\sqrt{P}$	80 MHz to 800 MHz $d = 1.2\sqrt{P}$	800 MHz to 2.5 GHz $d = 2.3\sqrt{P}$
0.01	0.12	0.12	0.12	0.23
0.1	0.38	0.38	0.38	0.73
1	1.2	1.2	1.2	2.3
10	3.8	3.8	3.8	7.3
100	12	12	12	23
NOTE 1: At 80 MHz and 800 MHz, the separation distance for the higher frequency range applies.				

For transmitters rated at a maximum output power not listed above, the recommended separation distance [**d**] in meters (m) can estimated using the equation applicable to the frequency of the transmitter, where **P** is the maximum output power rating of the transmitter in watts (w) according to the transmitter manufacturer.

NOTE

These guidelines may not apply in all situations. Electromagnetic propagation is affected by absorption and reflection from structures, objects and people

Compliant Cables and Accessories

WARNING
The use of accessories, transducers and cables other than those specified may result in increased emissions or decreased immunity performance of the equipment or system.

The table below lists cables, transducers, and other applicable accessories with which GE Medical Systems claims EMC compliance.

NOTE
Any supplied accessories that do not affect EMC compliance are not included.

Part Number	Description	Maximum Lengths
900770-001	MAC Pac Battery	NA
900995-002	Cam 14	NA
2016560-001	Cable Assembly Host Mac 5500	1.7m
2016560-003	Cable Assembly Host Mac 5500ST	5.4m
901142-001	Kit Cam 14 Resting W/AHA Adaptors	NA
901142-002	Kit Cam 14 Resting W/IEC Adaptors	NA
400073-001	Serial Comm. Cable 8 Pin Mini DIN	6.1m
416070-001	External Video Cable	1.8m
700520-002	Analog/TTL Interface Cable	3.0m
2007918-001	Treadmill Cable Mac 5500ST to T2000	6.0m
405535-006	Power Supply Cord US 13A 125V	3.0m
401855-001	Power Supply Cord European 10A 250V	2.5m
401855-002	Power Supply Cord British 10A 250V	2.5m
401855-003	Power Supply Cord Italian 10A 250V	2.5m
401855-004	Power Supply Cord Israeli 10A 250V	2.5m
401855-007	Power Supply Cord Swiss 10A 250V	2.5m
401855-008	Power Supply Cord Indian 10A 250V	2.5m
401855-010	Power Supply Cord Australian 10A 250V	2.5m
2005264-XXX	MAC 5500 External Modem Kit	NA
2018626-XXX	MAC 5500 Barcode Scanner Kit	NA
2018627-XXX	MAC 5500 Magnetic Card Reader Kit	NA
2014403-XXX	Mac 5500 Wireless Kit	NA
2023922-XXX	Mac 5500 Secure Wireless Kit	NA

For your notes

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